

Top assembly

Component placement, fitted-side orientation and 3D reference

ASSEMBLY NOTES

01 View from outside the top of the board. Use the PCB outline and connector edges to orient the board.

02 Reference plan is 1:1.36 at A3 / 100% print (170 mm board shown 125 mm wide). 3D illustration is not a dimensional drawing.

03 Teal outlines identify pad 1 / A1. Verify device polarity and pin numbering against the footprint and datasheet.

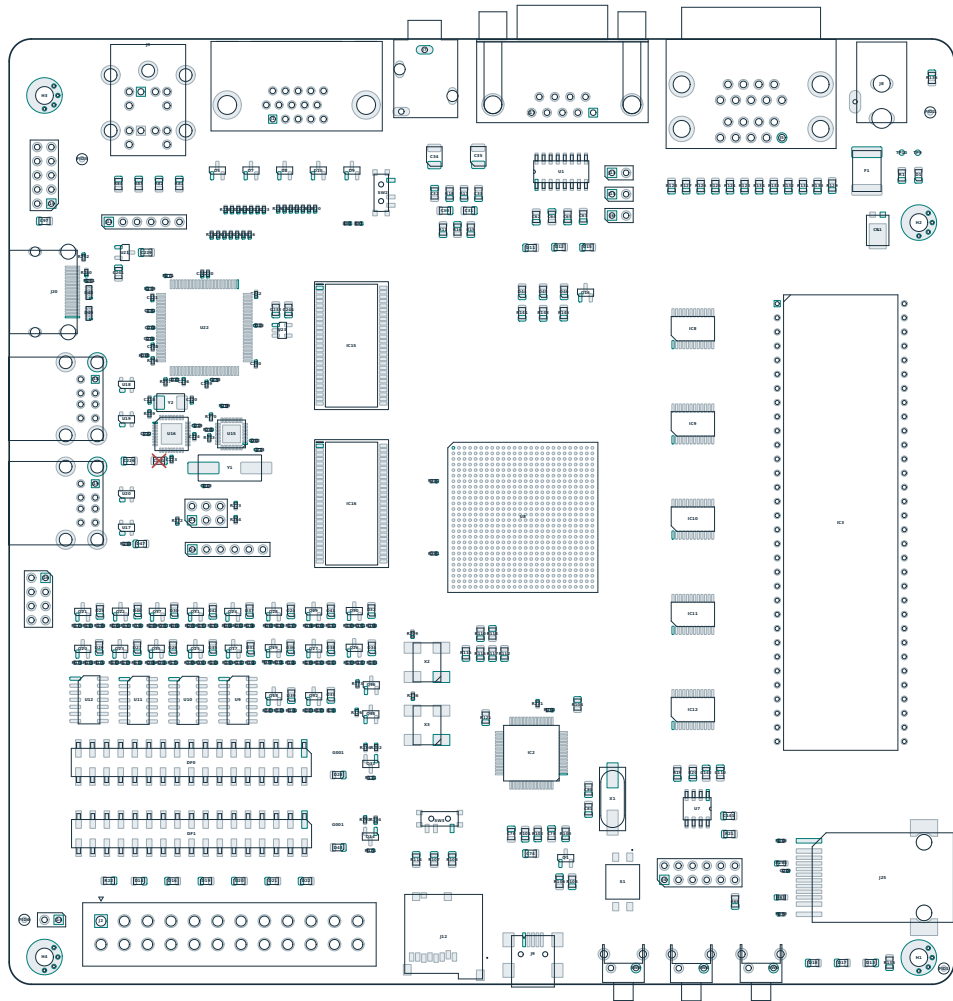
04 Red crosses mark DNP footprints. The BOM controls population and component values.

05 Drawings show the saved AmiCube revision, including the moved J25 Ethernet jack and the complete 68000 level-shifter interface.

06 IC15 and IC16 use independent 16-bit SDRAM buses. IC17 and IC18 complete the 68000 interface on the bottom side.

07 FID1-4 are on top; FID5-8 are on the bottom. Native footprints control fiducial geometry. Markers are excluded from the purchasing BOM.

REFERENCE PLAN / 1:1.36

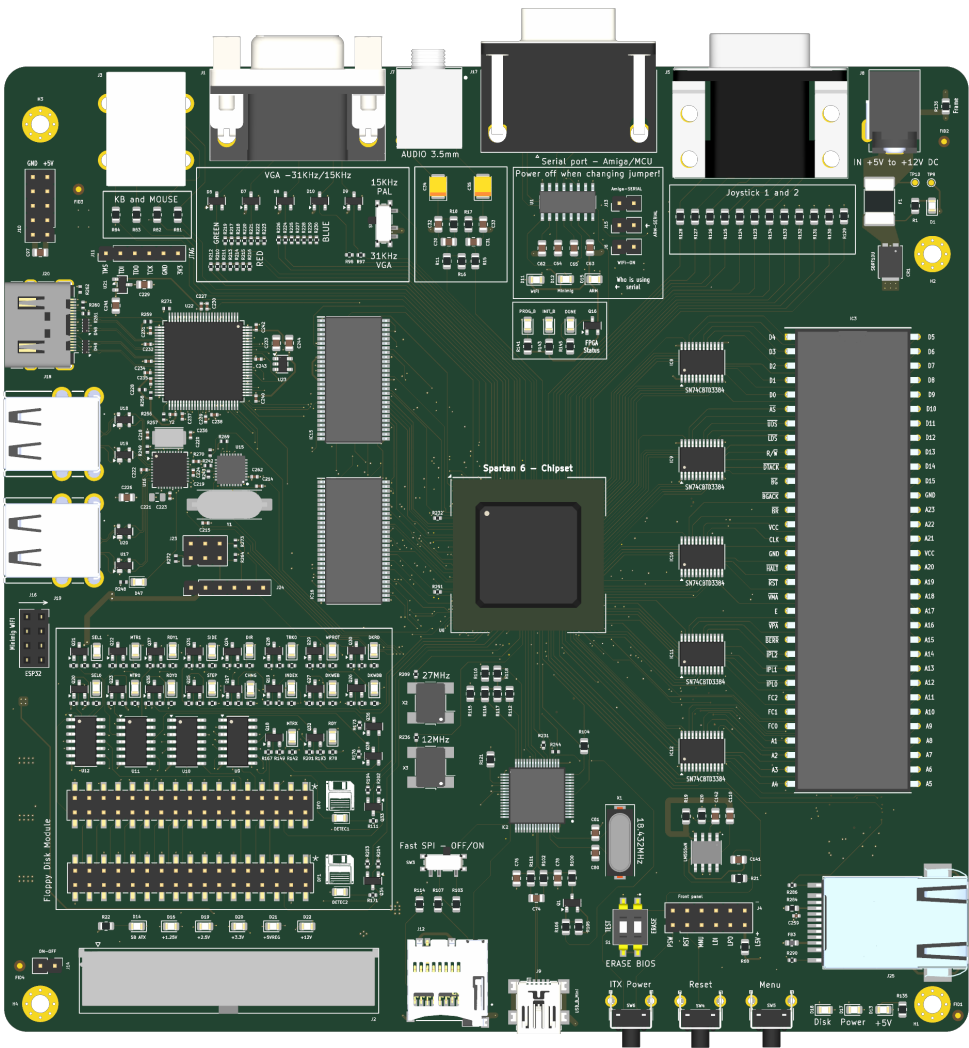


25 mm print scale check

FID1: X 298.050, Y 219.760 mm (native top view)

FID2: X 295.600, Y 65.800 mm (native top view)

3D ASSEMBLY VIEW



ASSEMBLY INVENTORY

Placement	Footprints	SMD attr.	DNP
Top side	352	320	1
Bottom side	314	304	20

KEY DEVICES

Reference	Role	Device
U8	FPGA / BGA676	XC6SLX100-FGG676
IC2	Control MCU	AT91SAM7S256D
U26	Ethernet controller	ENC624J600-I/PT

Bottom assembly

Component placement, fitted-side orientation and 3D reference

ASSEMBLY NOTES

01 View from outside the bottom of the board. Bottom drawing is mirrored left to right.

02 Reference plan is 1:1.36 at A3 / 100% print (170 mm board shown 125 mm wide). 3D illustration is not a dimensional drawing.

03 Teal outlines identify pad 1 / A1. Verify device polarity and pin numbering against the footprint and datasheet.

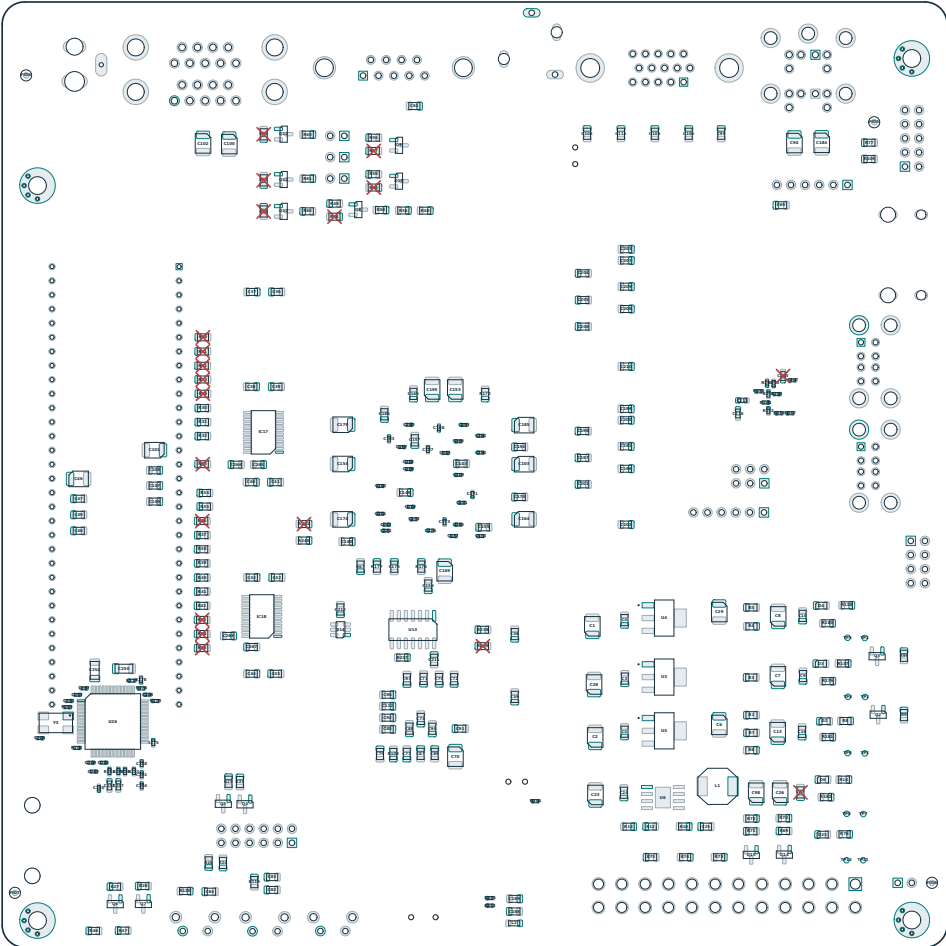
04 Red crosses mark DNP footprints. The BOM controls population and component values.

05 Drawings show the saved AmiCube revision, including the moved J25 Ethernet jack and the complete 68000 level-shifter interface.

06 IC15 and IC16 use independent 16-bit SDRAM buses. IC17 and IC18 complete the 68000 interface on the bottom side.

07 FID1-4 are on top; FID5-8 are on the bottom. Native footprints control fiducial geometry. Markers are excluded from the purchasing BOM.

REFERENCE PLAN / 1:1.36

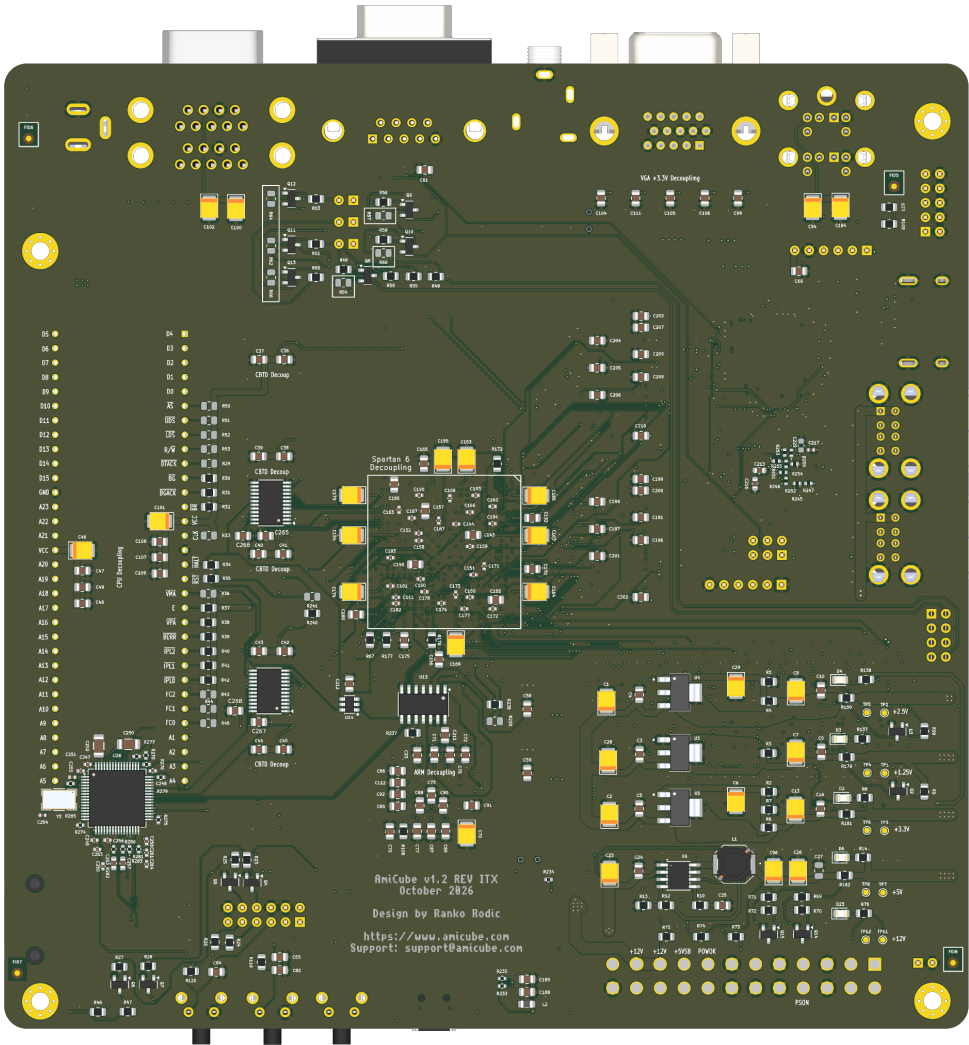


25 mm print scale check

FID5: X 143.020, Y 74.230 mm (native top view)

FID6: X 295.600, Y 65.800 mm (native top view)

3D ASSEMBLY VIEW



Frame0-CONNECTED MOUNTING HOLES

Ref	Hole	X	Y
H1	3.2	163.65	165.20
H2	3.2	163.65	33.02
H3	3.2	6.35	10.16
H4	3.2	6.35	165.10

Four 3.2 mm clearance holes. 170 × 170 mm outline with R4 corners; nominal thickness 1.6 mm.

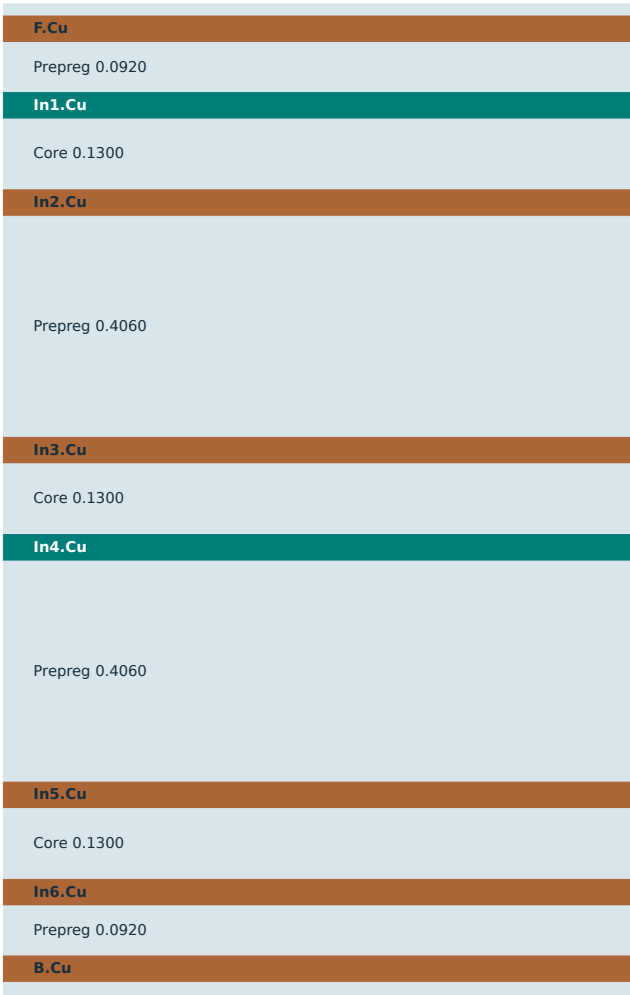
Coordinates are measured from the top-view upper-left outline tangent, +X right and +Y down. Bottom illustration is mirrored; this coordinate table remains in top-view coordinates.

Stackup & fabrication

Saved laminate definition, layer allocation and actual through-via inventory

8 LAYERS / NOMINAL 1.6 mm

Cross-section: thickness exaggerated



Layer	Material / construction	t (mm)	Er	Df	Function
F.Mask	Solder mask	0.01	—	—	Coating
F.Cu	Copper	0.035	—	—	Signals / components
dielectric 1	3313 RC57%	0.092	4.1	0.02	Insulation
In1.Cu	Copper	0.03	—	—	GND reference
dielectric 2	NP-155F core	0.13	4.17	0.02	Insulation
In2.Cu	Copper	0.03	—	—	Signals / power
dielectric 3	2 x 7628 RC49%	0.406	4.4	0.02	Insulation
In3.Cu	Copper	0.03	—	—	Signals / power
dielectric 4	NP-155F core	0.13	4.17	0.02	Insulation
In4.Cu	Copper	0.03	—	—	GND reference
dielectric 5	2 x 7628 RC49%	0.406	4.4	0.02	Insulation
In5.Cu	Copper	0.03	—	—	Signals / 3.3 V
dielectric 6	NP-155F core	0.13	4.17	0.02	Insulation
In6.Cu	Copper	0.03	—	—	Power / local GND
dielectric 7	3313 RC57%	0.092	4.1	0.02	Insulation
B.Cu	Copper	0.035	—	—	Signals / components / GND
B.Mask	Solder mask	0.01	—	—	Coating

Sum of saved thickness entries: 1.656 mm including masks; 1.636 mm without masks.

Laminate: NP-155F / JLC081611-3313. Saved copper: 0.035 mm outer / 0.030 mm inner.

Native copper-finish field: None. Manufacturing release remains pending.

THROUGH-VIA INVENTORY

Land Ø	Drill Ø	Annulus	Count
0.3	0.15	0.075	1180
0.4	0.2	0.100	304
0.5	0.2	0.150	42
0.5	0.25	0.125	3
0.6	0.3	0.150	2

FABRICATION REVIEW NOTES

Outline: 170 × 170 mm, R4 corners. Four 3.2 mm mounting holes. 1,531 routing vias; minimum recorded drill 0.15 mm. Mounting-ring drills are counted separately.

In1 and In4 carry the ground-reference pours. In6 includes split supply copper and local ground; do not assume an unbroken ground plane.

Confirm final stack, finish, via treatment and controlled-impedance requirements before fabrication. Archived production files predate the current circuit.

Routing & impedance

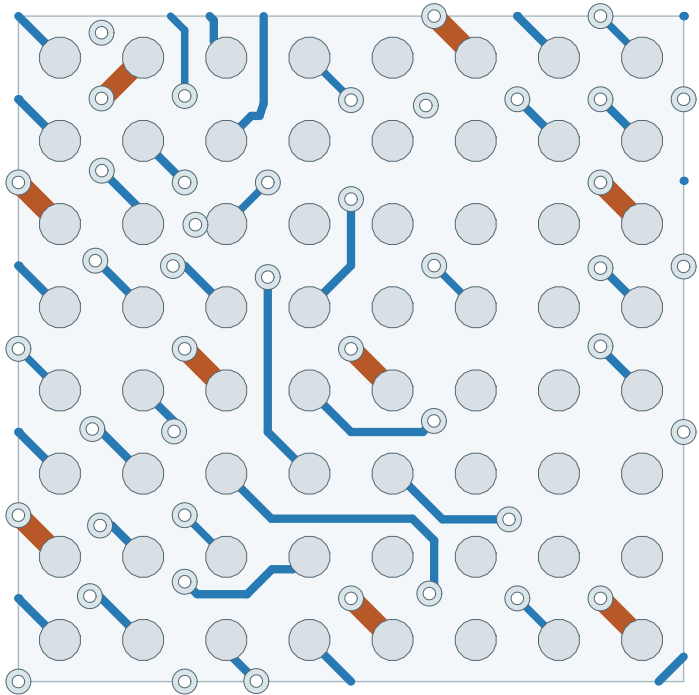
Current differential-pair targets and local BGA rules — main project

Circuit / class	Scope	Width	Gap	Target Zdiff	Notes
Digital data / control	All routing layers	0.100	—	Uncontrolled	Includes both SDRAM channels and clocks
BGA fanout / data	Under U8 / all Cu	0.100	—	Uncontrolled	Same signal width inside and outside FPGA fanout
U8 supply escape	U8 courtyard / all Cu	0.250	—	—	Local 1.25 V / 3.3 V; wider feeders allowed
USB differential	Outer layers	0.130	0.160	90 ohm	Host, hub, four downstream ports and service
USB hub pair	In2.Cu	0.130	0.170	90 ohm	In1 reference / In4 distant reference
HDMI TMDS	Outer layers	0.100	0.160	100 ohm	Three data pairs plus differential clock
Ethernet RX / TX	Outer layers	0.100	0.160	100 ohm	ENC624J600 to the current J25 location

Impedance values are nominal design targets; no new field-solver, TDR or timing qualification is implied.

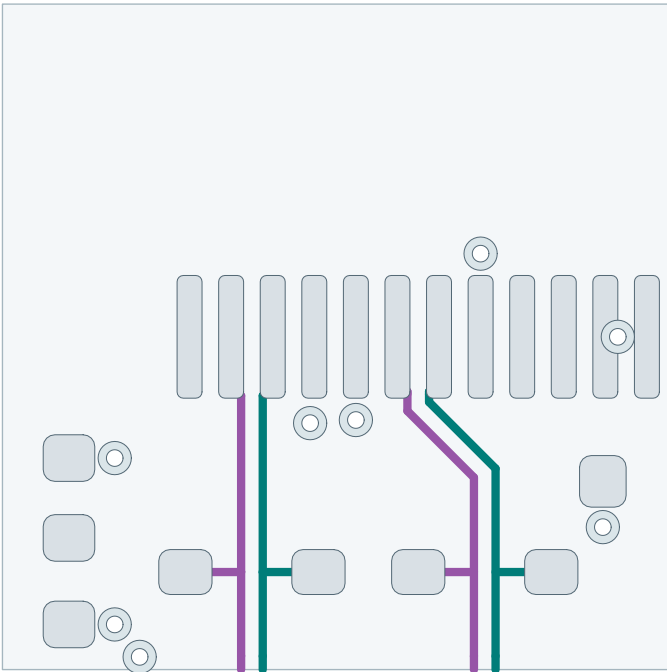
Pair-gap minimum: 0.15 mm. Optimum: 0.16 mm outer / 0.17 mm inner USB. Native custom rules govern.

A / BGA ESCAPE DETAIL



F.Cu / 11:1 — blue data, orange power

B / ETHERNET CONTROLLER DETAIL



B.Cu / 11:1 — top-view coordinates

Differential pair detail; other tracks omitted

REFERENCE PLANES & PAIR GEOMETRY



F.Cu references In1 ground. Bottom differential routes rely on local In6 ground. In2 USB uses In1 with In4 as the distant second reference.

In3 and In5 contain signals and power. In6 is split power / local ground. Check the actual copper beneath every high-speed route.

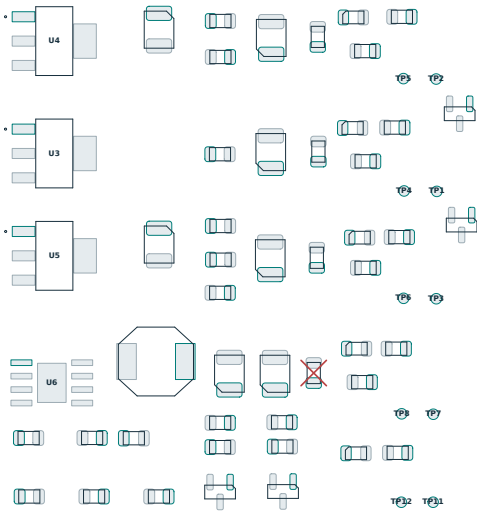
IC15 and IC16 have independent 16-bit buses. Their shared supplies do not make their clocks, address or command nets common.

Keep return paths continuous when editing. Width / gap rules are in AmiCube-v1.kicad_dru; FPGA timing and hardware tests remain pending.

Power & signal identification

Regulated-rail probe points, LED meaning and saved bus colours

REGULATOR / TEST-POINT LOCATOR



Bottom view / 1.4:1 / mirrored

REGULATED RAILS & INPUT

Nominal rail	Regulator	Indicator	Probe + / GND
+1.25V	U3	D16	TP1 / TP4
+2.5V	U4	D19	TP2 / TP5
+3.3V	U5	D20	TP3 / TP6
+5VREG	U6	D21	TP7 / TP8
12V-Supply	Input	D22 / D23	TP11 / TP12

All listed probe pairs are on the bottom. Additional top-side 12 V pair: TP10 (+) / TP9 (GND). Verify rail and ground before probing; labels are nominal values, not acceptance tolerances.

D16 / D19 / D20 / D21 indicate the labelled supplies. D44 / D45 / D46 display FPGA PROG_B, INIT_B and DONE circuit states. LED illumination does not qualify voltage, ripple or firmware operation.

EDITOR COLOUR CONVENTIONS

Clocks are yellow. The two SDRAM channels have separate palettes. Buses, supply rails and standalone signals retain their saved native colours. Colour does not change connectivity or routing dimensions.

VGA, HDMI and the two SDRAM interfaces retain distinct bus colours. The full saved netclass palette defines the individual supply rails and support signals.

BUS COLOUR KEY

68000 address	FPGA SPI	Joystick B	USB port 1 pair
68000 control	FPGA configuration	SD card	USB port 2 pair
68000 data	Floppy	SDRAM1 address	USB port 3 pair
Analogue audio	HDMI TMDS clock	SDRAM1 control	USB port 4 pair
Analogue video	HDMI TMDS data 0	SDRAM1 data	USB service pair
Clocks	HDMI TMDS data 1	SDRAM2 address	VGA blue data
Digital single signals	HDMI TMDS data 2	SDRAM2 control	VGA green data
Ethernet RX pair	HDMI blue data	SDRAM2 data	VGA red data
Ethernet TX pair	HDMI green data	System reset	Video control
Ethernet address	HDMI red data	USB host SPI	
Ethernet control	JTAG	USB host pair	
Ethernet data	Joystick A	USB hub pair	