

Top assembly

Component placement, fitted-side orientation and 3D reference

ASSEMBLY NOTES

01 View from outside the top of the board. Use the PCB outline and connector edges to orient the board.

02 Reference plan is 1:1 at A3 / 100% print. 3D illustration is not a dimensional drawing.

03 Teal outlines identify pad 1 / A1. Verify device polarity and pin numbering against the footprint and datasheet.

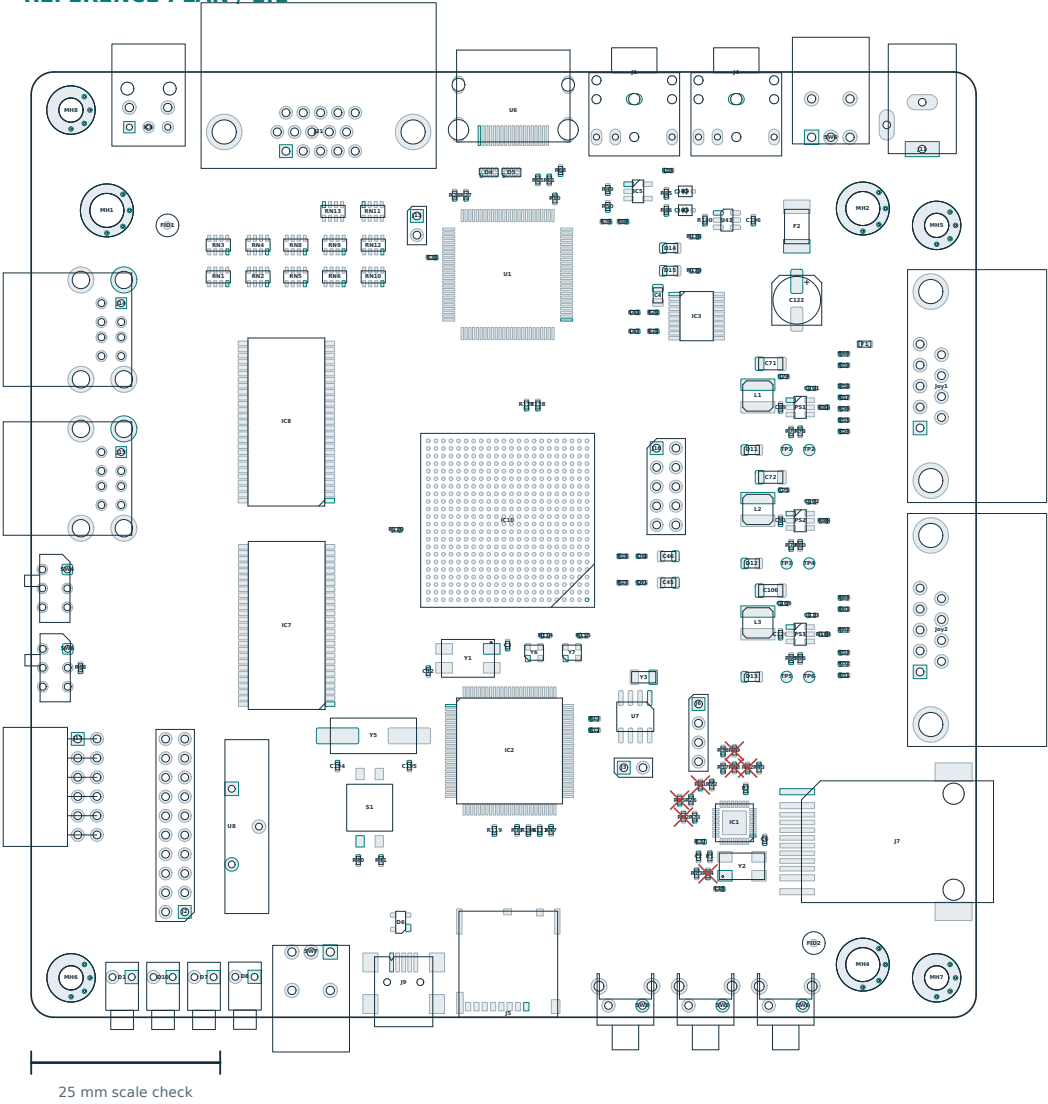
04 Red crosses mark DNP footprints. The BOM controls population and component values.

05 October 14: 19 ports/controls and 10 nearby parts repositioned; affected routes repaired. Drawings show current placement.

06 VGA DAC: 18 Bourns CAT16-4990F4LF arrays, each 4 x 499 ohm / 1%. Top: RN1-6 and RN8-13. Bottom: RN7 and RN14-18.

07 FID1/2 top and FID3/4 bottom: 1 mm copper, 3 mm mask opening, no paste. Board-only markers excluded from BOM and placement files.

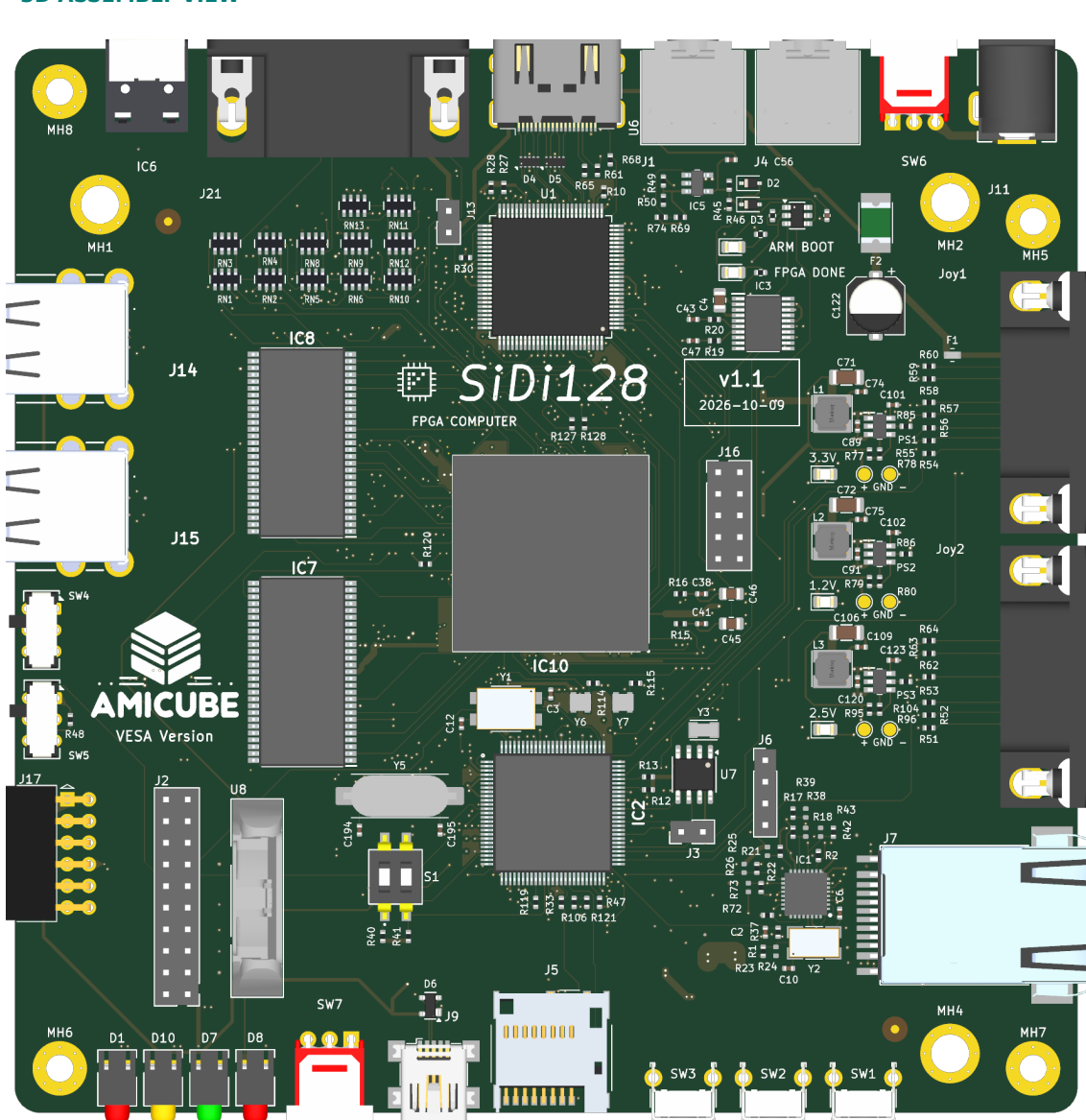
REFERENCE PLAN / 1:1



FID1: X 94.500, Y 86.500 mm (native top view)

FID2: X 180.000, Y 181.400 mm (native top view)

3D ASSEMBLY VIEW



ASSEMBLY INVENTORY

Placement	Footprints	SMD attr.	DNP
Top side	196	154	7
Bottom side	191	189	0

KEY DEVICES

Reference	Role	Device
IC10	FPGA / BGA484	10CL120YF484C8G
IC2	Control MCU	ATSAMV71N20B
IC1	Ethernet PHY	KSZ8061RNBW

Bottom assembly

Component placement, fitted-side orientation and 3D reference

ASSEMBLY NOTES

01 View from outside the bottom of the board. Bottom drawing is mirrored left to right.

02 Reference plan is 1:1 at A3 / 100% print. 3D illustration is not a dimensional drawing.

03 Teal outlines identify pad 1 / A1. Verify device polarity and pin numbering against the footprint and datasheet.

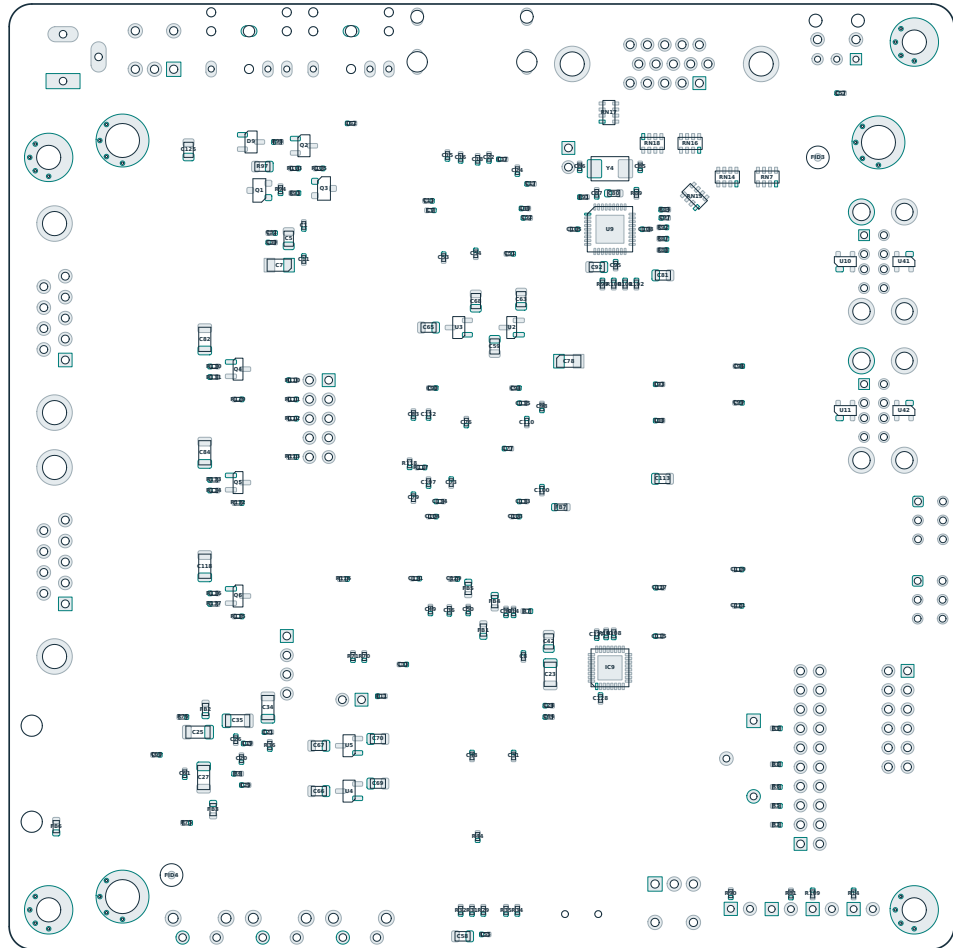
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REFERENCE PLAN / 1:1

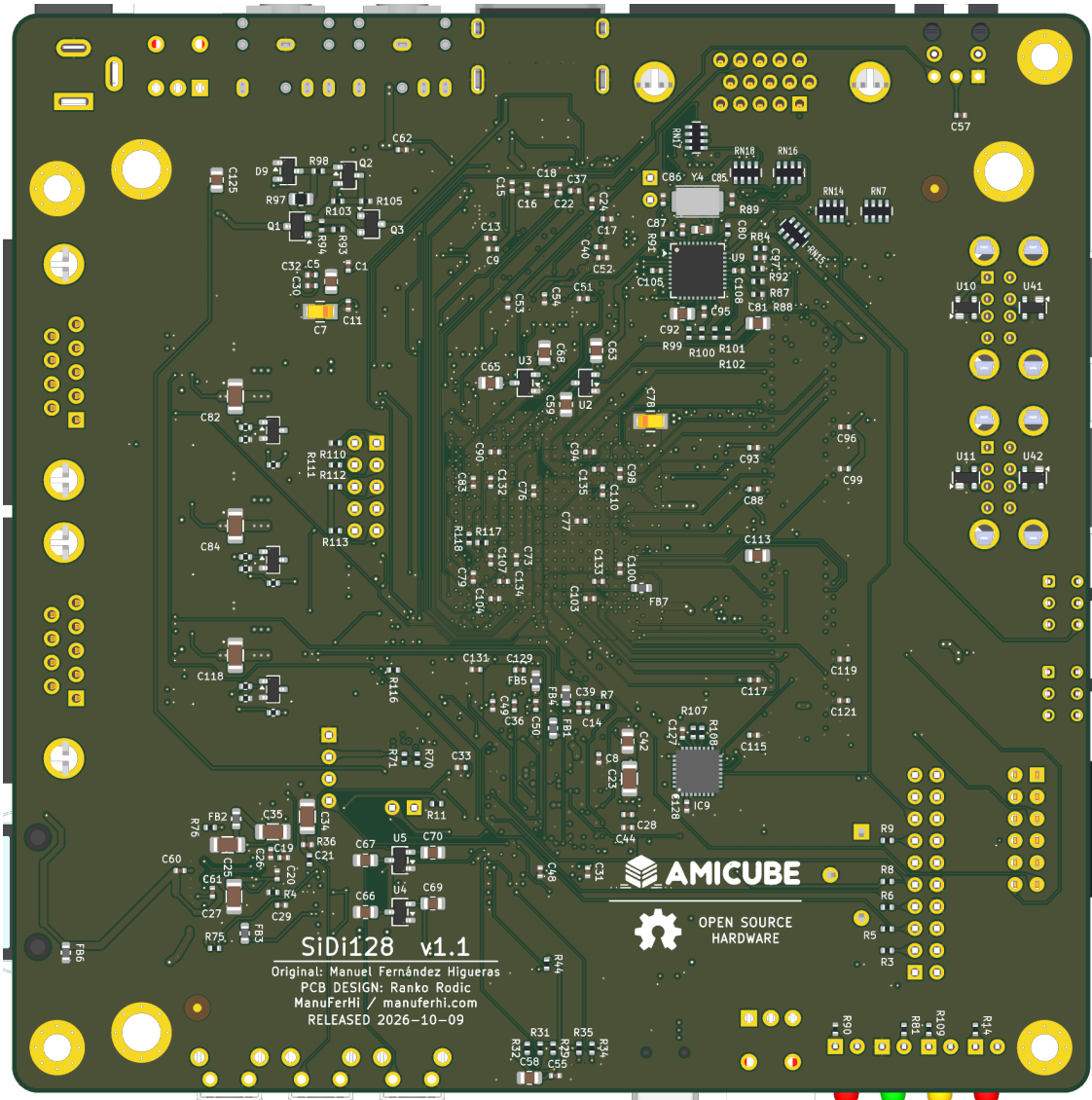


25 mm scale check

FID3: X 94.500, Y 86.500 mm (native top view)

FID4: X 180.000, Y 181.400 mm (native top view)

3D ASSEMBLY VIEW



GROUND-CONNECTED MOUNTING HOLES

Ref	Hole	X	Y
MH1	4.5	10.01	18.30
MH2	4.5	110.01	18.05
MH4	4.5	110.01	118.04
MH5	3.2	119.78	20.29

Ref	Hole	X	Y
MH6	3.2	5.28	119.79
MH7	3.2	119.78	119.79
MH8	3.2	5.26	5.04

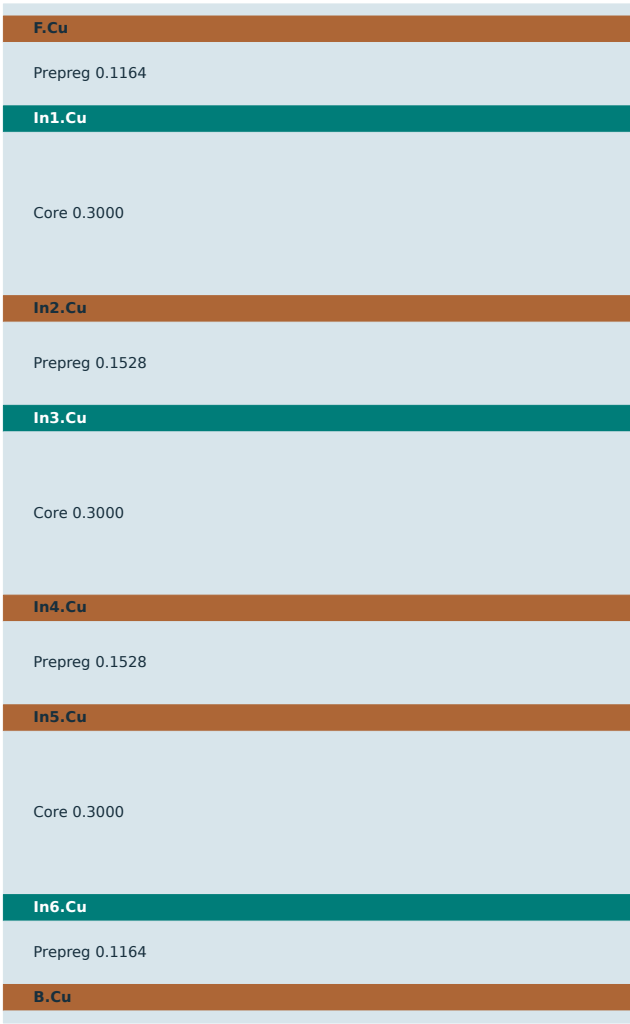
Coordinates are measured from the top-view upper-left outline tangent, +X right and +Y down. Bottom illustration is mirrored; this coordinate table remains in top-view coordinates.

Stackup & fabrication

Saved laminate definition, layer allocation and actual through-via inventory

8 LAYERS / NOMINAL 1.6 mm

Cross-section: thickness exaggerated



THROUGH-VIA INVENTORY

Land Ø	Drill Ø	Annulus	Count
0.35	0.15	0.100	832
0.45	0.2	0.125	900
0.5	0.25	0.125	52
0.55	0.3	0.125	3
0.6	0.3	0.150	100

Layer	Material / construction	t (mm)	Er	Df	Function
F.Mask	Solder mask	0.01524	—	—	Coating
F.Cu	Copper	0.035	—	—	Signals / components
dielectric 1	2116 RC54%	0.1164	4.16	0.016	Insulation
In1.Cu	Copper	0.0152	—	—	GND reference
dielectric 2	0.3mm core	0.3	4.41	0.016	Insulation
In2.Cu	Copper	0.0152	—	—	Signals
dielectric 3	2 x 1080 / RC67%	0.1528	3.91	0.016	Insulation
In3.Cu	Copper	0.0152	—	—	GND reference
dielectric 4	0.3mm core	0.3	4.41	0.016	Insulation
In4.Cu	Copper	0.0152	—	—	Signals / power
dielectric 5	2 x 1080 / RC67%	0.1528	3.91	0.016	Insulation
In5.Cu	Copper	0.0152	—	—	Signals
dielectric 6	0.3mm core	0.3	4.41	0.016	Insulation
In6.Cu	Copper	0.0152	—	—	GND reference
dielectric 7	2116 RC54%	0.1164	4.16	0.016	Insulation
B.Cu	Copper	0.035	—	—	Signals / components
B.Mask	Solder mask	0.01524	—	—	Coating

Sum of saved thickness entries: 1.63008 mm (including solder masks). Finish: ENIG.

Laminate family: NP-155F / selected JLC08161H-2116 profile. Copper: 0.035 outer / 0.0152 inner.

FABRICATION REVIEW NOTES

Outline: 125 × 125 mm, R3 corners. Minimum recorded through-via drill: 0.15 mm. Detailed PTH / NPTH holes and slots remain defined by the drill files.

Uploaded fabrication instructions require epoxy fill, planarize and copper-cap BOTH faces of all 1,887 routing vias. The coordinate map controls treatment; component holes, slots and NPTH stay open.

The order has no impedance-control / TDR requirement. Preserve the saved JLC08161H-2116 stack and nominal geometry. Two stencils: seven DNP resistors and four fiducials have no paste openings.

Routing & impedance

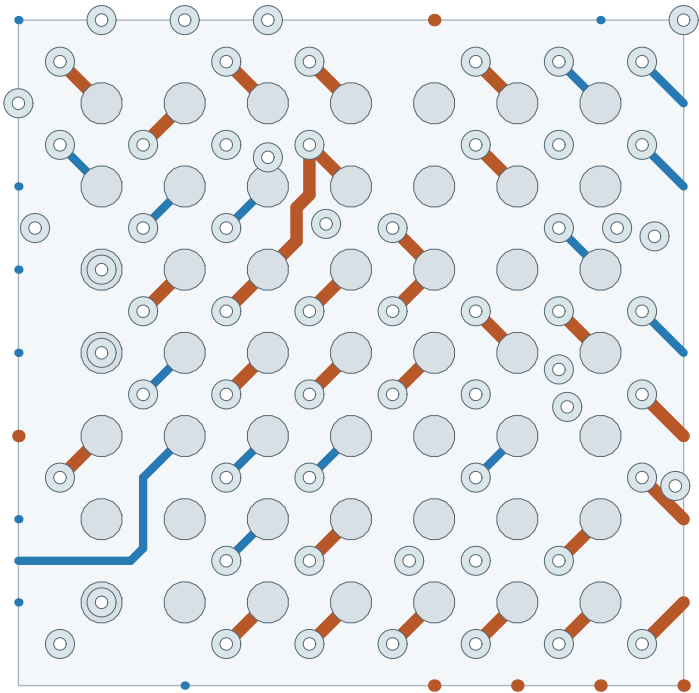
Current differential-pair targets and local BGA rules — main project

Circuit / class	Scope	Width	Gap	Target Zdiff	Notes
DATA_0P10	All routing layers	0.100	—	Uncontrolled	Single-ended data / control / clocks and RGB ladder
BGA_FANOUT / data	Under IC10, all Cu	0.100	—	Uncontrolled	Same signal width inside and outside FPGA fanout
BGA_POWER_FANOUT	Under IC10, all Cu	0.150	—	—	Local power 0.15; wider branches / trunks retained
USB90	F / In2 / B	0.160	0.150	90 ohm	Saved nominal geometry; endpoint exceptions apply
USB90	In5,Cu	0.184	0.126	90 ohm	Revised In3 / In6 reference; In4 corridor kept clear
HDMI_TMDS100	F	0.122	0.150	100 ohm	Saved nominal geometry; component-pitch exceptions
ETH_MDI100	F / In2 / B	0.122	0.150	100 ohm	Saved nominal geometry; local skew compensation

Impedance values are nominal design targets; the order has no impedance-control / TDR requirement. Local rules remain unchanged.

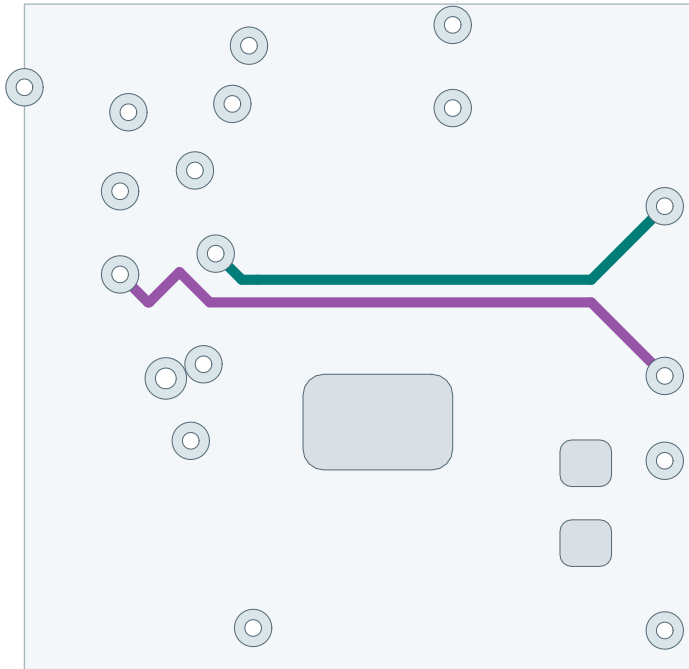
Port revision: HDMI routes 11.8103 mm / 12 mm limit; USB In5 routing and its In4 clearance corridor follow the moved ports.

A / BGA ESCAPE DETAIL



F.Cu / 11:1 — blue data, orange power

B / ETHERNET PHY DETAIL



B.Cu / 11:1 — top-view coordinates

TX_P teal / TX_N violet; other nets omitted

REFERENCE PLANES & PAIR GEOMETRY



F.Cu references In1 GND. B.Cu references In6 GND. In2 lies between In1 and In3 GND.

In4 is signal / power, not a ground plane. In5 pair calculations must include the revised reference geometry and intervening In4 copper.

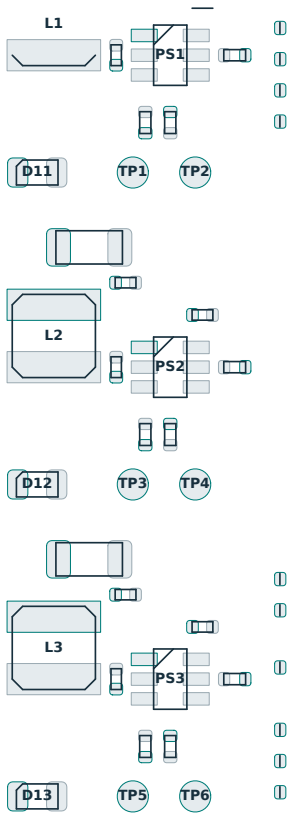
0.10 mm pair-skew limits are local routing targets where defined in the rules. They do not establish FPGA bus timing or system-level signal integrity.

Keep reference-plane continuity and existing return paths when editing. Detailed width and gap exceptions remain in SiDi128.kicad_dru.

Power & signal identification

Regulated-rail probe points, LED meaning and saved bus colours

REGULATOR / TEST-POINT LOCATOR



Top view / 2.75:1

THREE REGULATED RAILS

Nominal rail	Regulator	Indicator	Probe + / GND
3.3V	PS1	D11 / Green	TP1 / TP2
1.2V	PS2	D12 / Red	TP3 / TP4
2.5V	PS3	D13 / Yellow	TP5 / TP6

The LEDs are powered from 3.3V and switched by the monitored rails through Q4–Q6. Illumination indicates rail presence; it is not a calibrated voltage-window or ripple test. Loss of 3.3V can extinguish all three indicators.

Use the paired GND test point with each positive probe point. Compare the measured voltage to the regulator design requirements; the nominal labels above are not acceptance tolerances.

EDITOR COLOUR CONVENTIONS

Clocks are yellow. Standalone data/control signals are white in PCB Editor. Buses have their own colours; individual supply rails also have distinct colours. Colour classes change presentation, not electrical width or clearance.

VGA RGB colours continue through the 499-ohm arrays: RGB_R/G/B inputs, LADDER_R/G/B nodes and ROUT/GOUT/BOUT outputs share each channel colour on both board sides. GND retains its common ground colour.

BUS COLOUR KEY

- AUDIO DIGITAL
- CLOCKS
- CONTROL
- ETHERNET PAIRS
- EXPANSION
- FPGA CONFIG
- FPGA JTAG
- HDMI AUDIO
- HDMI CONTROL
- HDMI PAIRS
- HDMI VIDEO
- I2C
- I2S
- JOYSTICK 0
- JOYSTICK 1
- MCU JTAG
- QSPI
- RGB BLUE
- RGB GREEN
- RGB RED
- RMII
- SDRAM 1
- SDRAM 2
- SD CARD
- SPI
- UART
- USB CONTROL
- USB PAIRS
- VIDEO SYNC