Top assembly

Component placement, fitted-side orientation and 3D reference

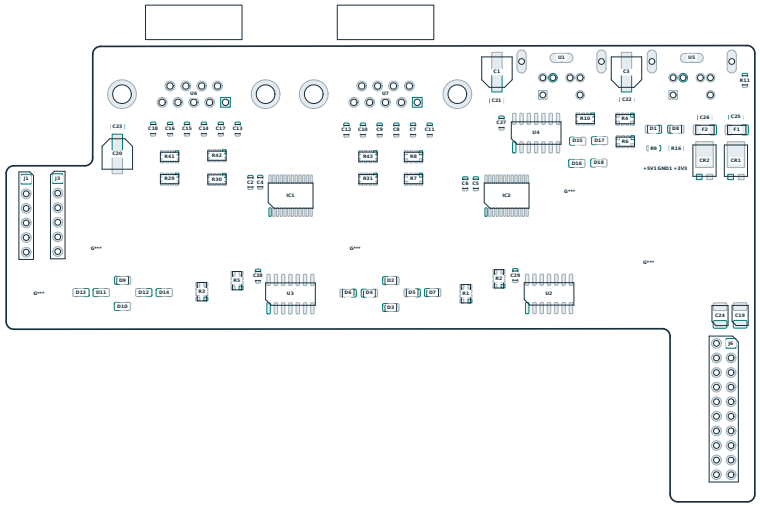
ASSEMBLY NOTES

01 View from outside the top of the board. Use connector edges to orient the board.

02 Teal identifies pad 1 / A1. Red crosses mark DNP footprints. Confirm polarity from the footprint and datasheet.

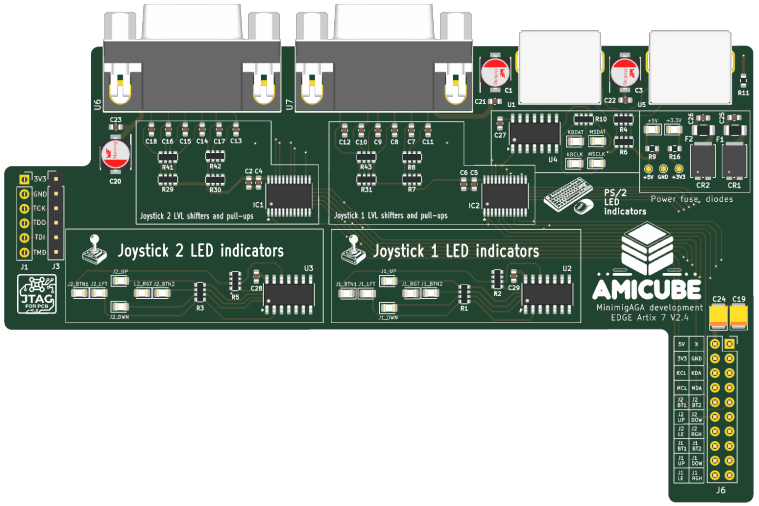
03 The component table controls values and population. The 3D view is illustrative; use the scale below for the plan.

REFERENCE PLAN



25 mm scale check / plan 0.76:1

3D ASSEMBLY VIEW



130.32 × 79.44 mm outline

ASSEMBLY INVENTORY

Placement	Footprints	SMD	DNP
Top side	89	74	0
Bottom side	6	0	0

Saved pads and fabrication outlines form the reference plan. Component values, connector pin maps and source notes are in documentation/index.html.

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2.4 • generated 2026-10-16 • source c3f4478de0cd

Units: mm. Source CAD governs. Regenerate after design changes.

Bottom assembly

Component placement, fitted-side orientation and 3D reference

ASSEMBLY NOTES

01 View from outside the bottom of the board. Bottom plan is mirrored.

02 Teal identifies pad 1 / A1. Red crosses mark DNP footprints. Confirm polarity from the footprint and datasheet.

03 The component table controls values and population. The 3D view is illustrative; use the scale below for the plan.

REFERENCE PLAN

25 mm scale check / plan 0.76:1

3D ASSEMBLY VIEW

130.32 × 79.44 mm outline

ASSEMBLY INVENTORY

Placement	Footprints	SMD	DNP
Top side	89	74	0
Bottom side	6	0	0

Saved pads and fabrication outlines form the reference plan. Component values, connector pin maps and source notes are in documentation/index.html.

Layer stackup and fabrication

Source project settings. Dimensions and fabrication parameters come from the saved PCB.

Layer	Type	Material	mm
F.SilkS	Top Silk Screen	—	—
F.Paste	Top Solder Paste	—	—
F.Mask	Top Solder Mask	—	0.01
F.Cu	copper	—	0.035
dielectric 1	prepreg	FR4	0.1
In1.Cu	copper	—	0.035
dielectric 2	core	FR4	1.24
In2.Cu	copper	—	0.035
dielectric 3	prepreg	FR4	0.1
B.Cu	copper	—	0.035
B.Mask	Bottom Solder Mask	—	0.01
B.Paste	Bottom Solder Paste	—	—
B.SilkS	Bottom Silk Screen	—	—

Saved board parameters

Property	Saved value
Outline	130.32 × 79.44 mm
Board thickness	1.6 mm
Copper layers	4
Footprints	95
Track/arc items	827
Vias	175

Saved routing rules / mm

Class	Clearance	Track	Via/drill
Default	0.2	0.2	0.6/0.3

These drawings record the source design. Confirm material, layer stack and fabrication capabilities against the native project before manufacture.

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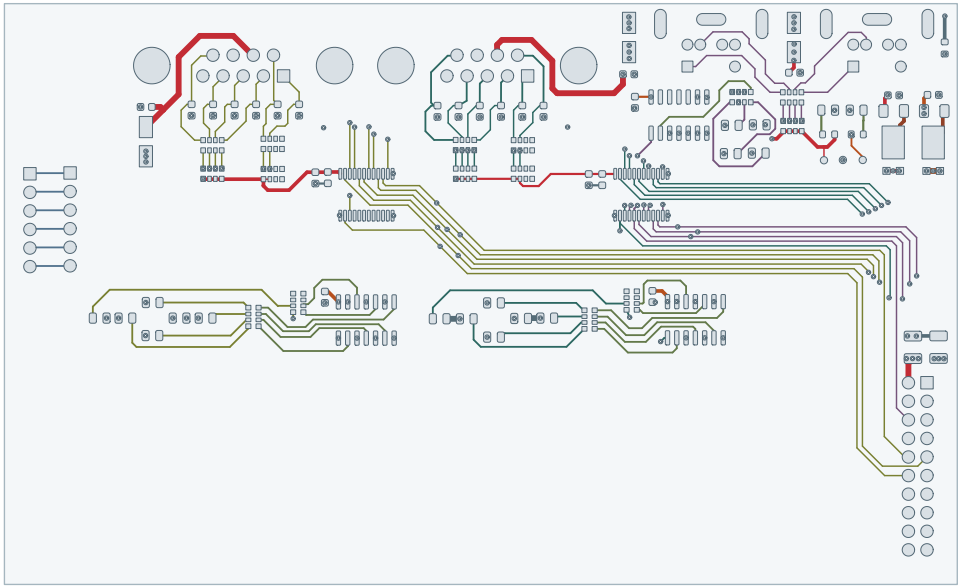
Units: mm. Source CAD governs. Regenerate after design changes.

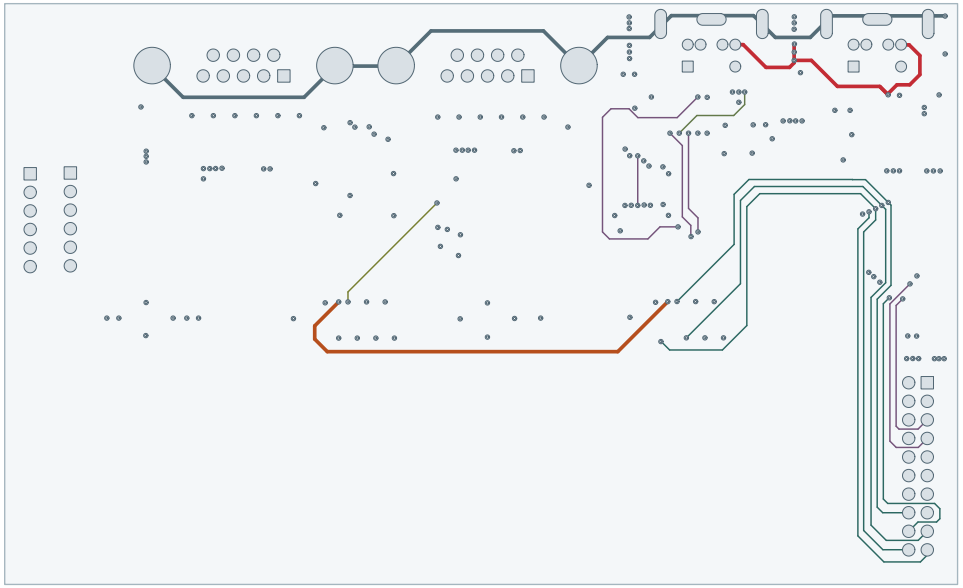
Routing guide

Outer copper from saved tracks, pads and vias. Filled zones are omitted for clarity.

Front copper



Back copper / through-board view



Colours identify net function. Grey pads and vias retain the saved geometry. Use native PCB layers for inner copper, zone fills and fabrication output.

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Units: mm. Source CAD governs. Regenerate after design changes.

Power and signal identification

Shared functional colour families for schematic labels and PCB copper.

GROUND	2
POWER 5V	2
POWER 3V3	2
POWER CONTROL	2
JOYSTICK 1	24
JOYSTICK 2	24
PS2	16
INDICATORS	18
EXPANSION	6

Follow each signal through the hierarchy by its global net label. Bus aliases summarize cross-sheet signal groups; the HTML guide lists every alias and colour assignment.

PCB Editor: Appearance → Objects → Net colours → All. Colour-only VIS_ classes preserve the original track, via and clearance rules.

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2.4 • generated 2026-10-16 • source c3f4478de0cd

Units: mm. Source CAD governs. Regenerate after design changes.