

Top assembly

Component placement, fitted-side orientation and native 3D reference

ASSEMBLY NOTES

01 View from outside the top of the board. Use the PCB outline and connector edges to orient the board.

02 Reference plan is 1:1.36 at A3 / 100% print (170 mm board shown 125 mm wide). 3D illustration is not a dimensional drawing.

03 Teal outlines identify pad 1 / A1. Verify device polarity and pin numbering against the footprint and datasheet.

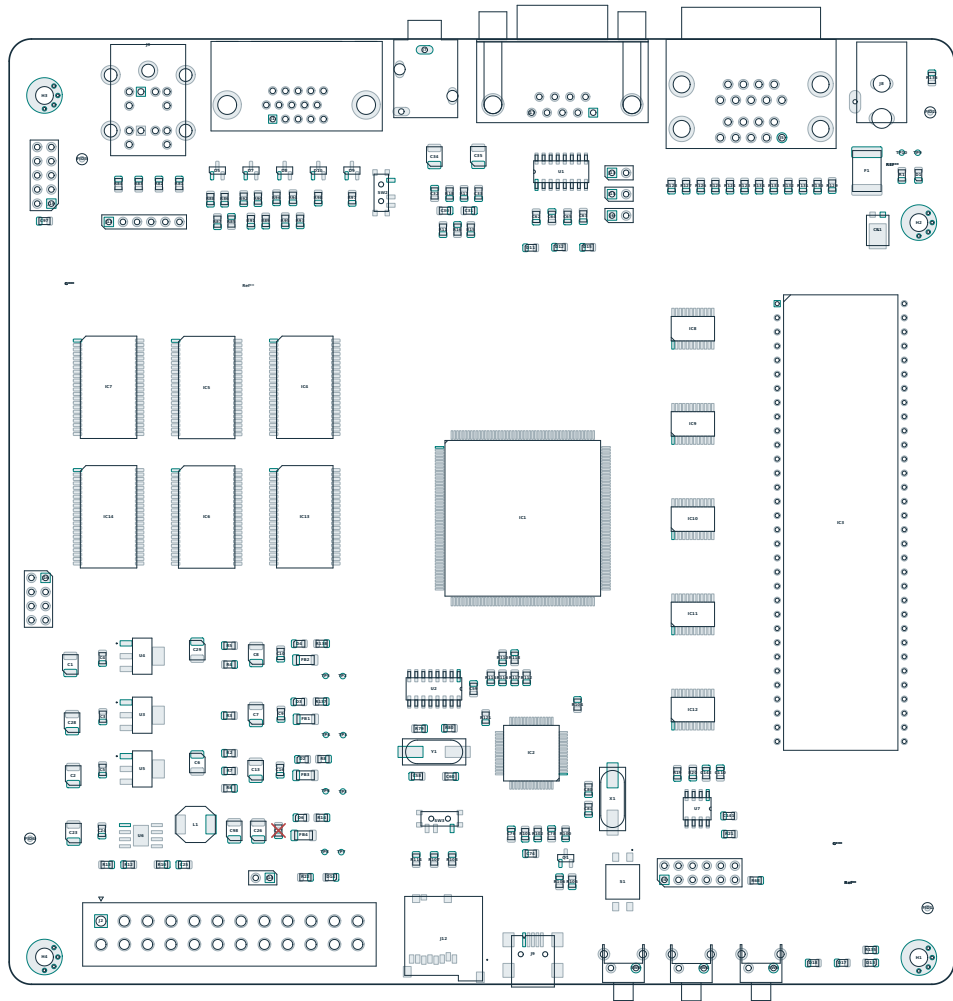
04 Red crosses mark footprints whose saved value is DNP. The source has 18 such options; native DNP flags are not set.

05 IC1 is Spartan-3 XC3S400. IC3 is the physical MC68000. IC8-12 provide the five-device bus translation interface.

06 IC4-7 / IC13-14 are six SRAM devices: shared 16-bit data bus, 19 address signals and six separate chip selects.

07 FID1-4 are on top; FID5-8 are on the bottom. Native footprints control geometry; graphics and fiducials are not purchased parts.

REFERENCE PLAN / 1:1.36

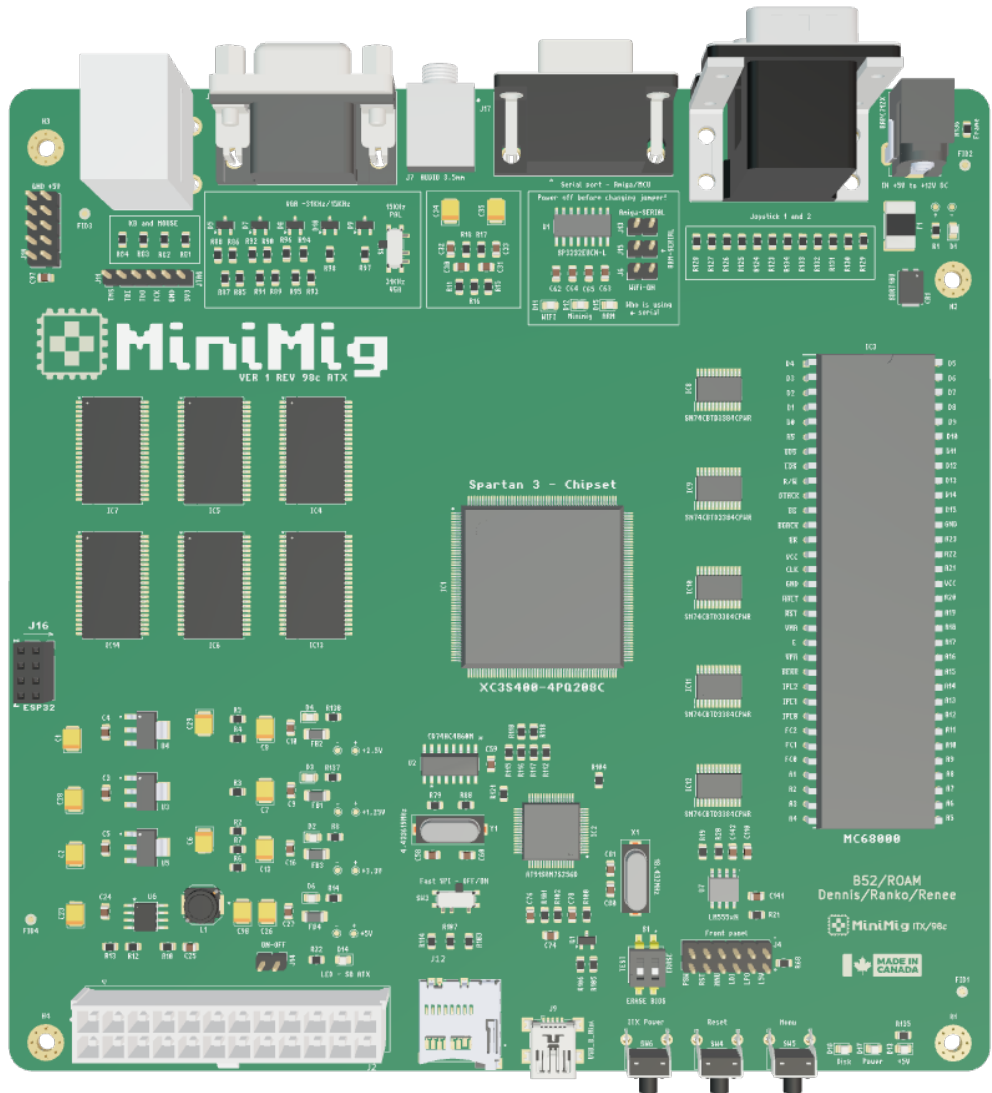


25 mm print scale check

FID1: X 295.110, Y 208.910 mm (native top view)

FID2: X 295.600, Y 65.800 mm (native top view)

3D ASSEMBLY VIEW



ASSEMBLY INVENTORY

Placement	Footprints	SMD attr.	DNP value
Top side	217	172	1
Bottom side	175	175	17

KEY DEVICES

Reference	Role	Device
IC1	FPGA / PQ208	XC3S400-4PQ208C
IC2	Control MCU	AT91SAM7S256D
IC3	Processor / DIP64	MC68000

Bottom assembly

Component placement, fitted-side orientation and native 3D reference

ASSEMBLY NOTES

01 View from outside the bottom of the board. Bottom drawing is mirrored left to right.

02 Reference plan is 1:1.36 at A3 / 100% print (170 mm board shown 125 mm wide). 3D illustration is not a dimensional drawing.

03 Teal outlines identify pad 1 / A1. Verify device polarity and pin numbering against the footprint and datasheet.

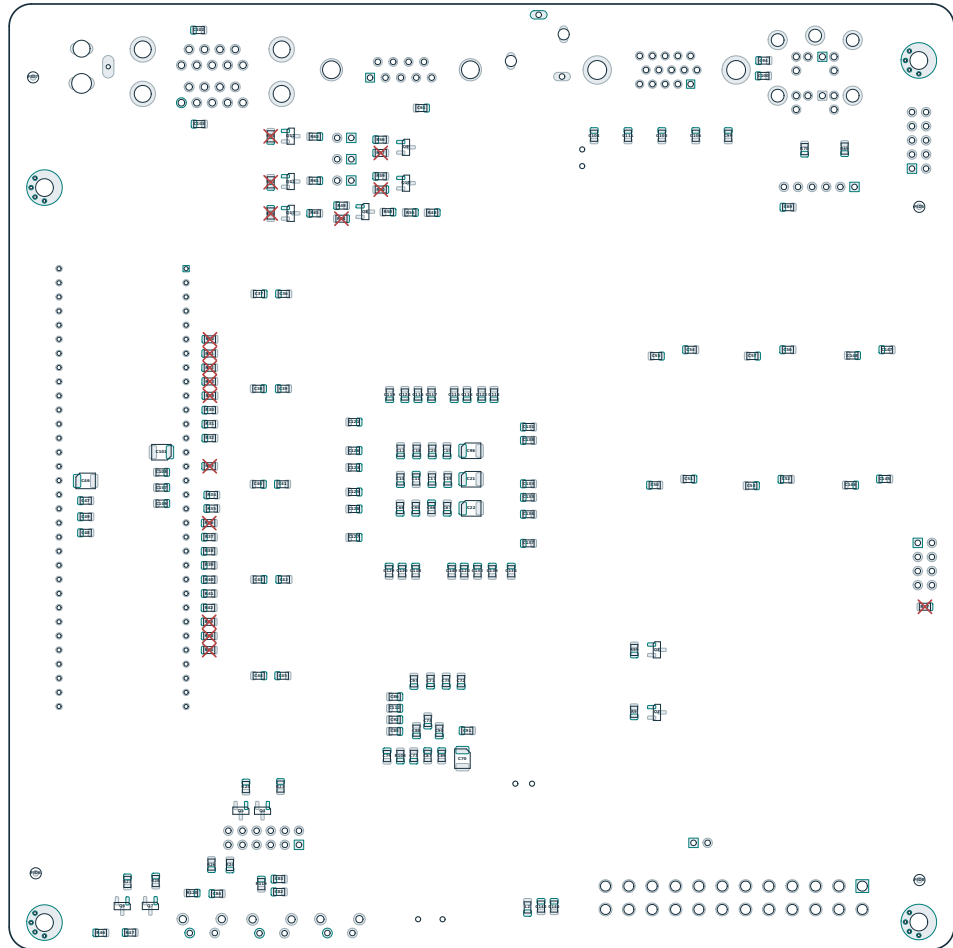
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REFERENCE PLAN / 1:1.36

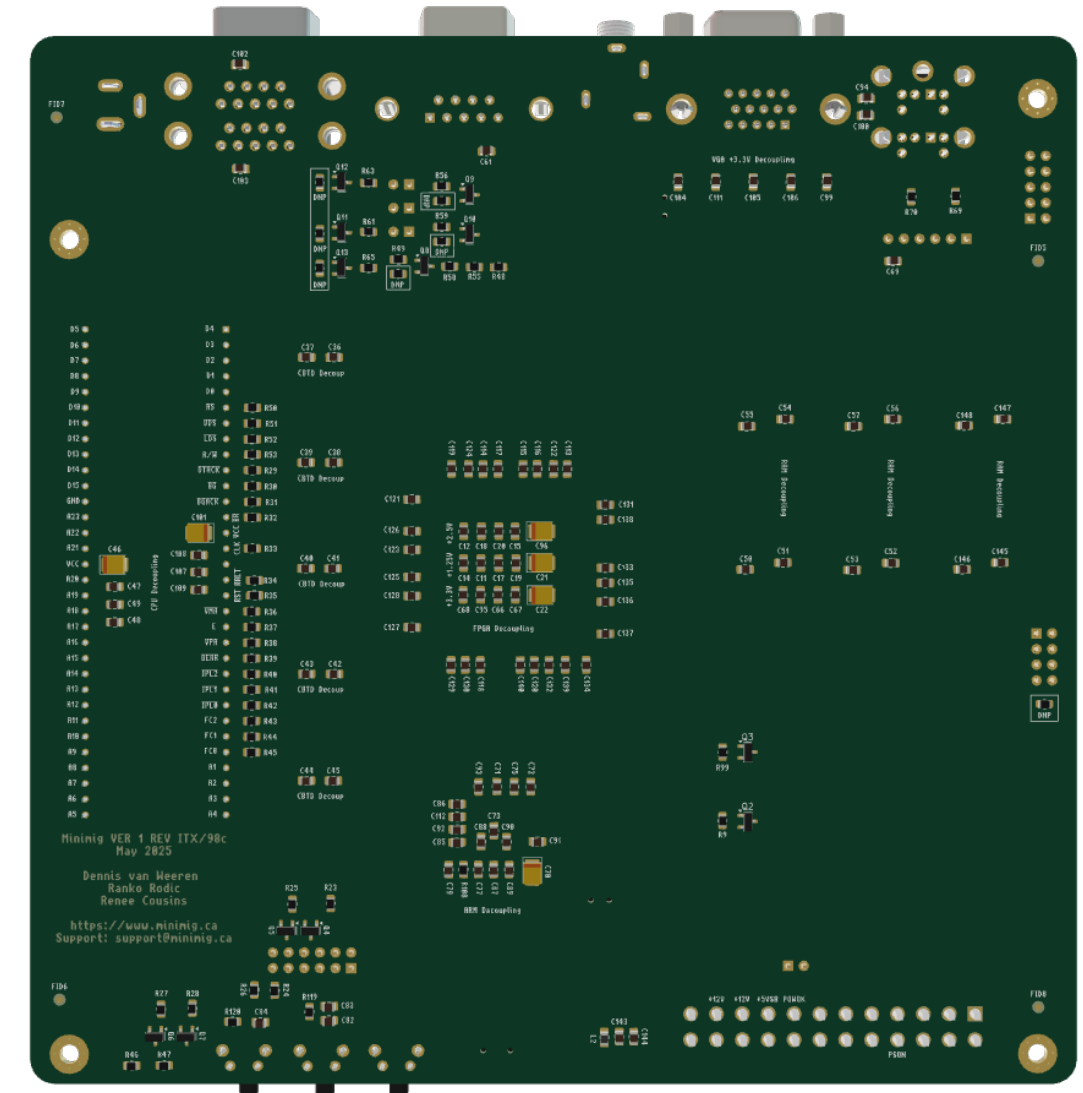


25 mm print scale check

FID5: X 136.170, Y 89.080 mm (native top view)

FID6: X 295.120, Y 208.940 mm (native top view)

3D ASSEMBLY VIEW



Frame0-CONNECTED MOUNTING HOLES

Ref	Hole	X	Y
H1	3.2	163.65	165.20
H2	3.2	163.65	33.02
H3	3.2	6.35	10.16
H4	3.2	6.35	165.10

Four 3.2 mm clearance holes. 170 × 170 mm outline with R4 corners; nominal thickness 1.6 mm.

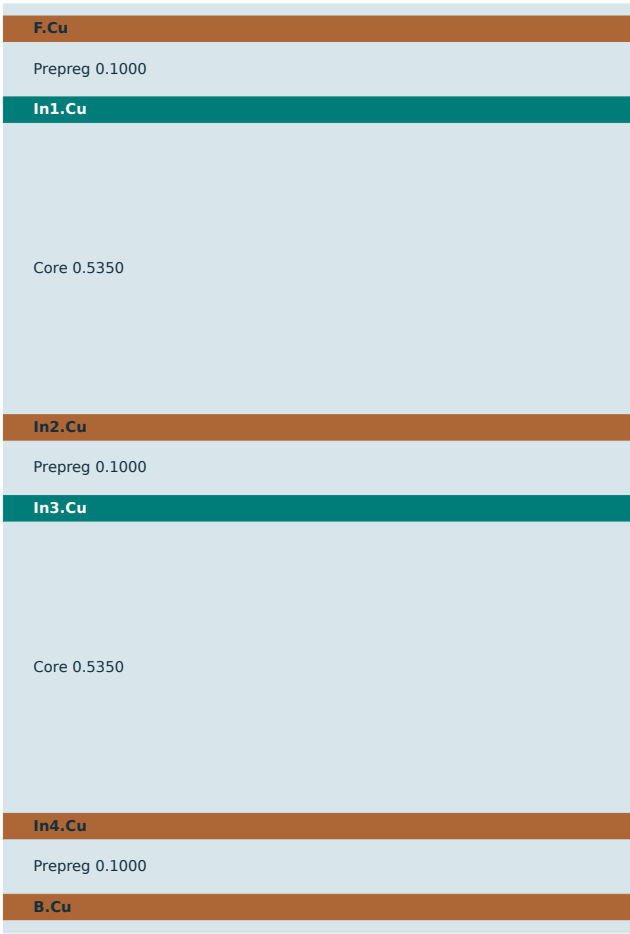
Coordinates are measured from the top-view upper-left outline tangent, +X right and +Y down. Bottom illustration is mirrored; this coordinate table remains in top-view coordinates.

Stackup & fabrication

Saved laminate definition, layer allocation and actual through-via inventory

6 LAYERS / NOMINAL 1.6 mm

Cross-section: thickness exaggerated



Layer	Material / construction	t (mm)	Er	Df	Saved role
F.Mask	Solder mask	0.01	—	—	Coating
F.Cu	Copper	0.035	—	—	Signals / power
dielectric 1	FR4	0.1	4.5	0.02	Insulation
In1.Cu	Copper	0.035	—	—	GND reference
dielectric 2	FR4	0.535	4.5	0.02	Insulation
In2.Cu	Copper	0.035	—	—	Signals / power
dielectric 3	FR4	0.1	4.5	0.02	Insulation
In3.Cu	Copper	0.035	—	—	GND reference
dielectric 4	FR4	0.535	4.5	0.02	Insulation
In4.Cu	Copper	0.035	—	—	Signals / power
dielectric 5	FR4	0.1	4.5	0.02	Insulation
B.Cu	Copper	0.035	—	—	GND label / routed signals
B.Mask	Solder mask	0.01	—	—	Coating

Sum of saved thickness entries: 1.600 mm including masks; 1.580 mm without masks.

Laminate: generic FR4, Er 4.5 / Df 0.02. Saved copper: 0.035 mm on all six copper layers.

Native copper-finish field: None. No specific laminate brand or finished impedance is recorded.

Layer names describe design intent. B.Cu is named GND but contains routed signal copper; inspect actual return paths and pours rather than assuming an unbroken plane.

THROUGH-VIA INVENTORY

Land Ø	Drill Ø	Annulus	Count
0.45	0.2	0.125	767

FABRICATION REVIEW NOTES

Outline: 170 × 170 mm, R4 corners. Four 3.2 mm mounting holes. 767 routing vias; recorded drill 0.20 mm. Component and mounting-hole drills are separate.

Confirm stack, surface finish, drill capability and final fabrication output before manufacture. This guide records the saved design and does not certify fabrication readiness.

Routing & impedance

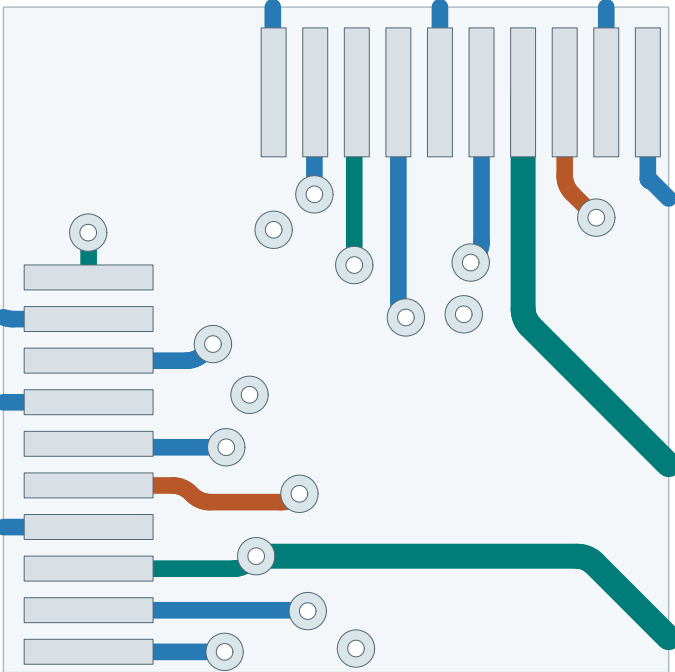
Saved widths, native copper details and the scope of the original routing rules

Circuit / class	Scope	Width	Gap	Target Zdiff	Saved design evidence
MC68000 translated bus	Recorded tracks	0.200	—	Not specified	49 used channels through IC8-12
Asynchronous SRAM	Recorded tracks	0.200	—	Not specified	Six devices share address and 16-bit data
VGA RGB / sync	Recorded tracks	0.200	—	Not specified	Four resistor-DAC bits per colour
USB service D+ / D—	Recorded tracks	0.200	—	Not specified	Mini-B J9 to ARM IC2; VBUS is unconnected
Default netclass	Project rule	0.250	0.250	Not specified	Diff-pair width 0.200; no board-specific Z target
Power nets	Recorded tracks	0.200–3.000	—	Not specified	Widths vary along the saved power routes
Minimum track width	Project rule	0.200	—	—	Default clearance 0.150 mm; one saved netclass

Widths above come from saved copper or the Default class. The project contains no per-interface impedance target.

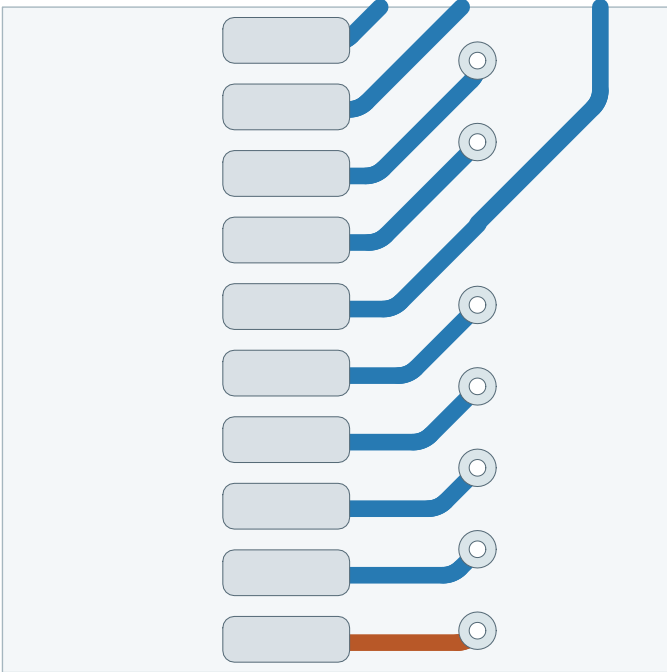
Drawing colours identify power and signals; they do not add netclasses, routing constraints or timing qualification.

A / SPARTAN-3 LEAD ESCAPE



F.Cu / 11:1 — blue data, orange power

B / SRAM BUS DETAIL



F.Cu / 11:1 — true saved arc geometry

Local IC4 region; top-view coordinates

REFERENCE PLANES & PAIR GEOMETRY



Illustration only — not to scale

In1 and In3 are labelled ground reference. F.Cu, In2 and In4 carry signals and power. B.Cu has a GND name and also contains routed signals.

The six asynchronous SRAM devices share RAM_D0–15 and RAM_A1–19. RAM_SELO–5 select devices individually; there is no SDRAM clock interface.

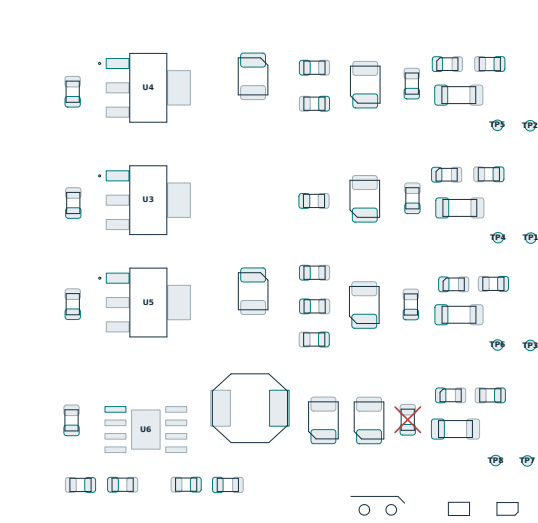
Native curved traces are preserved in the detail drawings. Visual separation does not establish skew, matched lengths or controlled impedance.

Keep return paths and supply decoupling intact when editing. This appendix records geometry; ERC, DRC and hardware qualification are separate reviews.

Power & signal identification

Regulated-rail probe points, LED meaning and a consistent drawing colour key

REGULATOR / TEST-POINT LOCATOR



Top view / 1.4:1

TP1 / TP4: 1.25 V

TP2 / TP5: 2.5 V

TP3 / TP6: 3.3 V

TP7 / TP8: 5 V

First = rail, second = GND.

REGULATED RAILS & INPUT

Nominal rail	Regulator	Indicator	Probe + / GND
+1.25V	U3	D3	TP1 / TP4
+2.5V	U4	D4	TP2 / TP5
+3.3V	U5	D2	TP3 / TP6
+5VREG	U6	D6	TP7 / TP8
12V-Supply	Input	D1	TP10 / TP9

All listed probe pairs are on top. TP10 (+12 V) / TP9 (GND) sit beside the barrel input. The board generates its operating rails; labels are nominal values, not acceptance tolerances.

D14 indicates ATX standby. U7 / 5VSB form the ATX control circuit. Mini-USB VBUS is unconnected. J10 is an auxiliary +5VREG / GND header, despite its saved Spare I/O value.

EDITOR COLOUR CONVENTIONS

The saved project has one Default netclass, with transparent native colour fields. The colour key below belongs to these drawings and the presentation; it does not modify PCB-editor settings.

Power, memory, processor and peripheral paths use distinct drawing colours. Named nets and pin connectivity remain the authority; colour is an aid to reading.

BUS COLOUR KEY / DOCUMENTATION

- Power rails
- MC68000 interface
- FPGA / ARM control
- Stereo audio
- Ground / return
- Shared SRAM bus
- Video / sync
- Joystick / PS/2 / serial

Nominal input: 12 V through J2 ATX or J8 barrel. Select the intended power source; simultaneous-source operation is not specified.