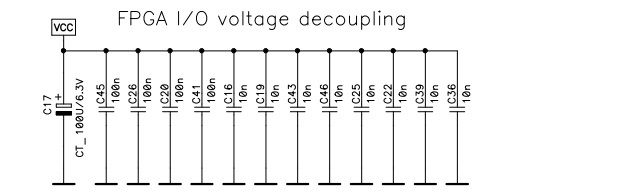
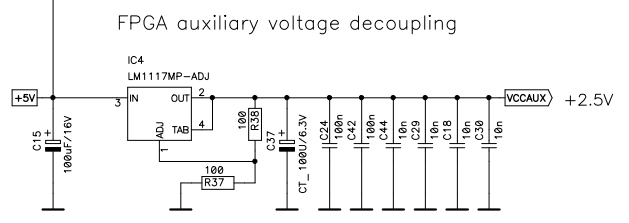
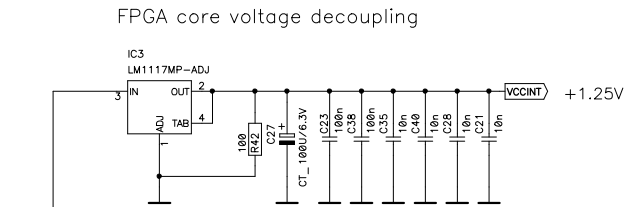
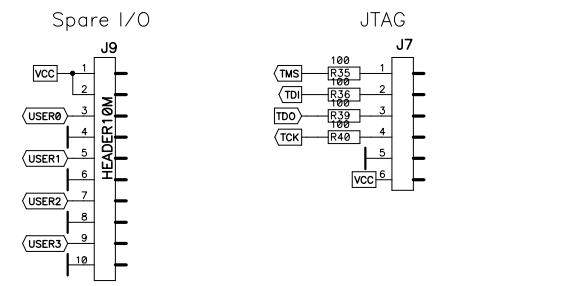
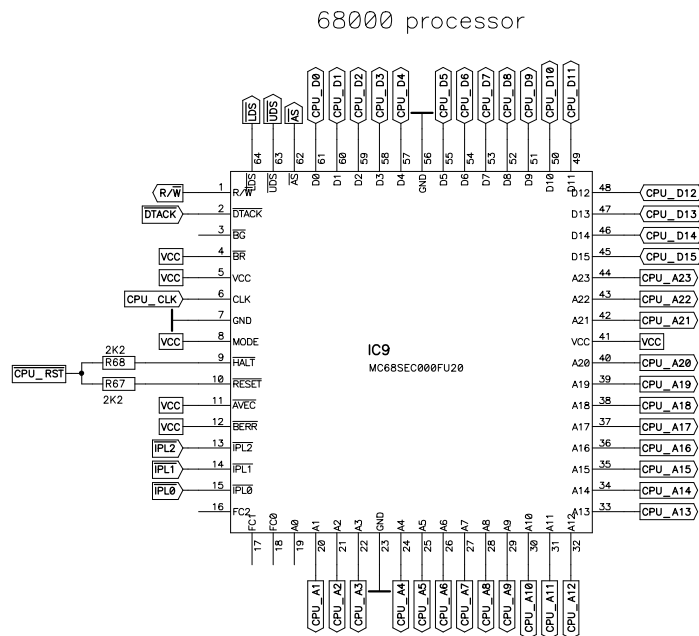


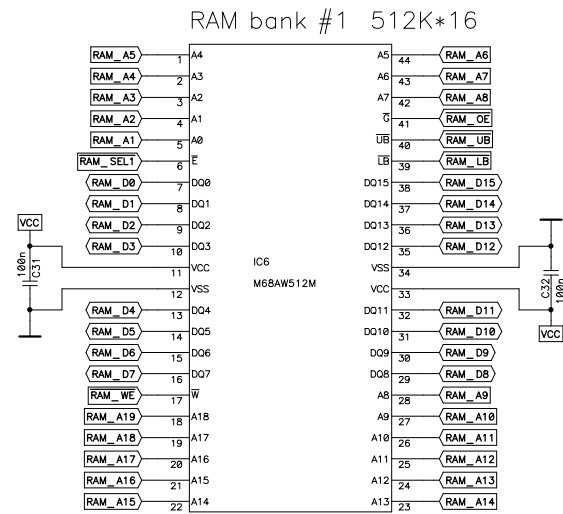
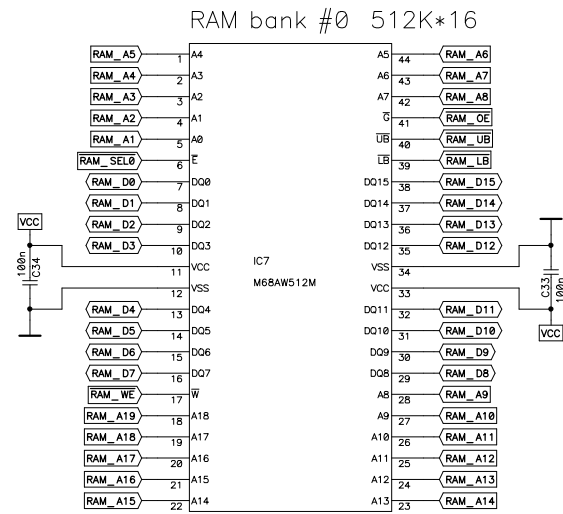
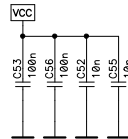
PATCH needed to get rev 1 board working:  
Disconnect net SPI\_DOUT from pin 81 of FPGA.  
Connect net SPI\_DOUT to pin 19 of FPGA (net USER3).  
REASON:  
Pin 81 is an output during FPGA config that blocks SPI to MMC during startup.



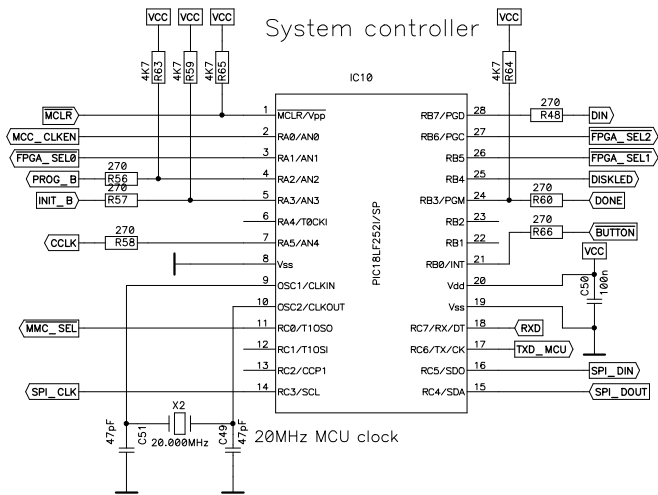
Title			MINIMIG REV 1.0		
Size	Number		Rev		
A2	SPARTAN POWER		2		
Date	03-10-2007		Drawn by Dennis van Weeren		
Filename	Minimig1		Sheet 1 of 3		



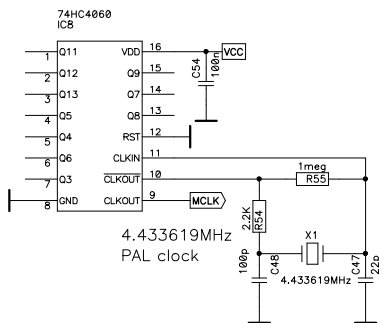
68000 decoupling



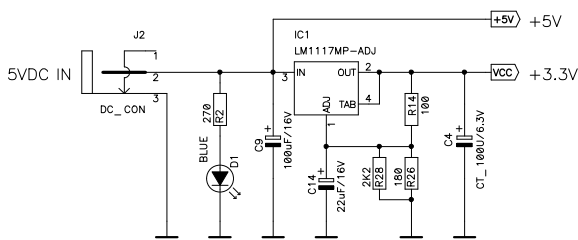
Title MINIMIG REV 1.0		
Size A2	Number 68000 FOREVER & RAM	Rev 2
Date 03-10-2007	Drawn by Dennis van Weeren	
Filename Minimig1	Sheet 2	of 3



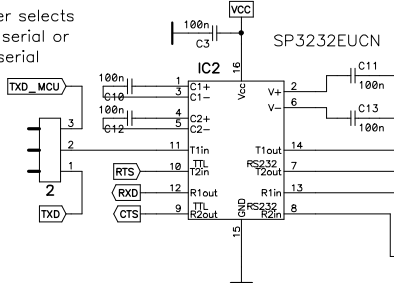
### Clock generator



### Main power supply

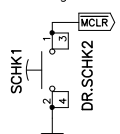


jumper selects  
FPGA serial or  
MCU serial

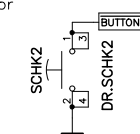


Serial port

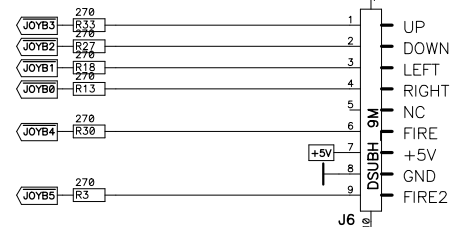
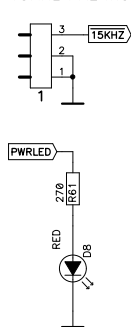
Programmers button



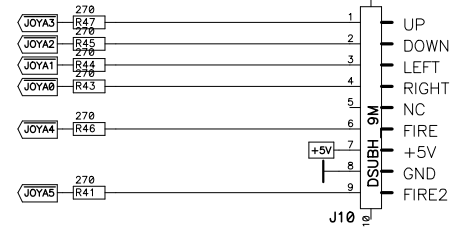
Button selects menu



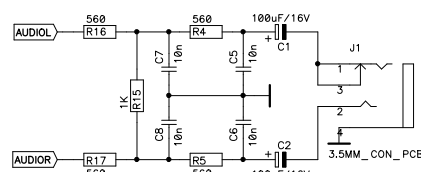
jumper selects  
31KHz VGA mode or  
15KHz PAL mode



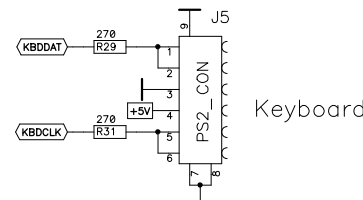
Joystick 1



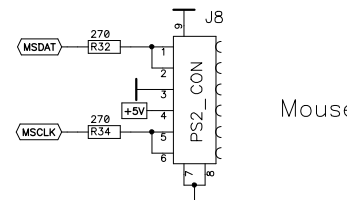
Joystick 0



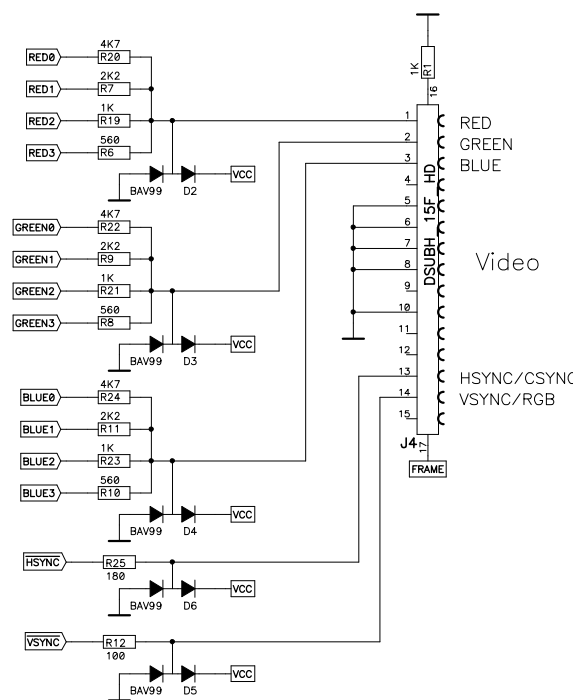
Audio



Keyboard



Mouse

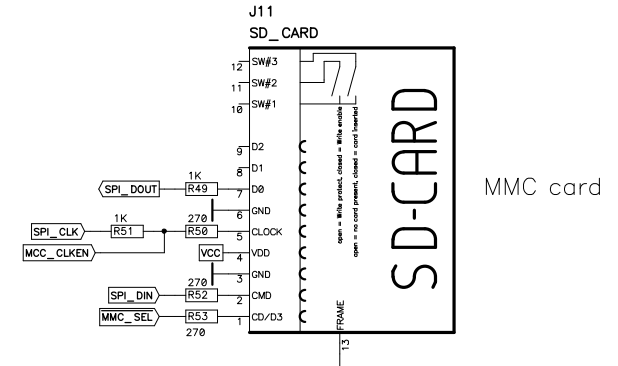


RED  
GREEN  
BLUE

Video

HSYNC/CSYNC  
VSYNC/RGB

in 15kHz mode:  
VSYNC = high (scart RGB enable)  
HSYNC = composite sync



MMC card

Title MINIMIG REV 1.0		
Size A2	Number I/O GALORE	Rev 2
Date 03-10-2007	Drawn by Dennis van Weeren	
Filename Minimig1	Sheet 3	of 3