System overview

Power and programmable logic

Sheet 02

{B_CIRCUITS1} {B_CIRCUITS1}

Controllers and interfaces

Sheet 11

{B_CIRCUITS2} {B_CIRCUITS2}

Board guide and engineering reference

Sheet 18

Hierarchical buses name the cross-sheet signals. Global labels continue each exact native net.

Open documentation/index.html for the board guide, connector maps and validation records.

BUS {B_ROOT}

B_CIRCUITS1, B_CIRCUITS2

Precision-Arrays / Minimig.ca

Sheet: /
File: AmiCube-MistITX.kicad_sch

Title: MIST ITX / sheet 1

Size: A4 | Date: 2026-10-16 | Rev: V1R9

KiCad E.D.A. 10.0.7 | Id: 1/23

Power and programmable logic

Input protection and switching regulator

Sheet 03

{B_POWER_INPUT} {B_POWER_INPUT}

ATX supply, front panel and status

Sheet 04

{B_ATX_POWER} {B_ATX_POWER}

Core and auxiliary supplies

Sheet 05

{B_CORE_AUX_POWER} {B_CORE_AUX_POWER}

3.3 V and 5 V supplies

Sheet 06

{B_LOGIC_POWER} {B_LOGIC_POWER}

FPGA power units

Sheet 07

{B_FPGA_POWER} {B_FPGA_POWER}

FPGA support and decoupling

Sheet 08

{B_FPGA_SUPPORT} {B_FPGA_SUPPORT}

FPGA configuration, clocks and JTAG

Sheet 09

{B_FPGA_CONTROL} {B_FPGA_CONTROL}

FPGA SDRAM interface and memory

Sheet 10

{B_MEMORY} {B_MEMORY}

Hierarchical buses name the cross-sheet signals. Global labels continue each exact native net.

Open documentation/index.html for the board guide, connector maps and validation records.

{B_CIRCUITS1}

BUS {B_CIRCUITS1}

B_POWER_INPUT, B_ATX_POWER, B_CORE_AUX_POWER, B_LOGIC_POWER, B_FPGA_POWER, B_FPGA_SUPPORT, B_FPGA_CONTROL, B_MEMORY

Precision-Arrays / Minimig.ca

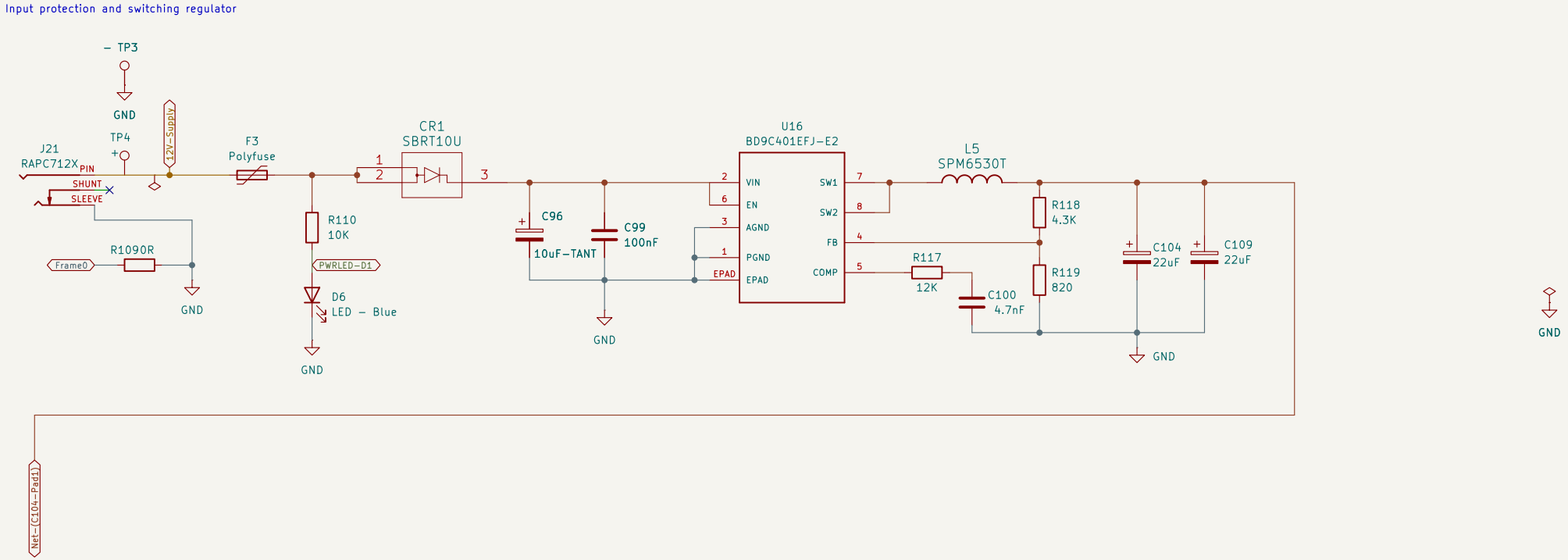
Sheet: /Power and programmable logic/
File: Circuits1.kicad_sch

Title: MIST ITX / sheet 2

Size: A4 | Date: 2026-10-16 | Rev: V1R9

KiCad E.D.A. 10.0.7 | Id: 2/23

Input protection and switching regulator



{B_POWER_INPUT}

BUS {B_POWER_INPUT}

12V-Supply, Frame0, GND, Net-(C104-Pad1)

Precision-Arrays / Minimig.ca

Sheet: /Power and programmable logic/Input protection and switching regulator/
File: power_input.kicad_sch

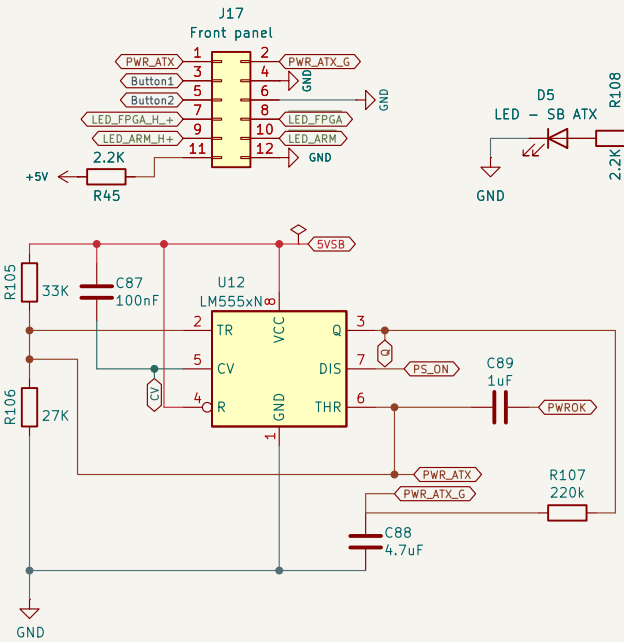
Title: MIST ITX / sheet 3

Size: A4 | Date: 2026-10-16 | Rev: V1R9

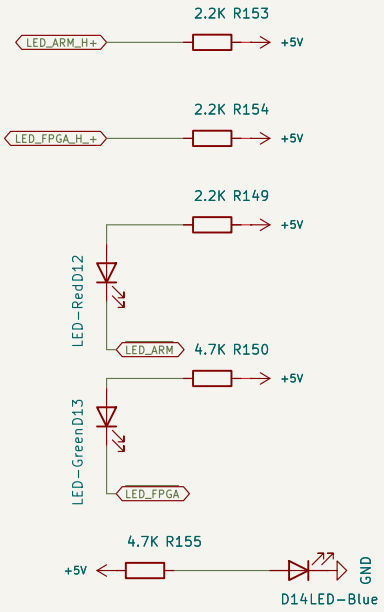
KiCad E.D.A. 10.0.7 | Id: 3/23

ATX supply, front panel and status

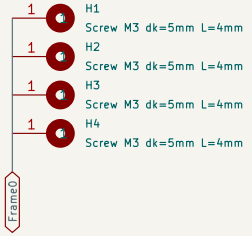
ATX supply and front panel



Status indicators



Mounting, fiducials and artwork



{B_ATX_POWER}

BUS {B_ATX_POWER}

12V-Supply, +5V, Button1, Button2, Frame0, GND, LED_ARM, LED_FPGA

Precision-Arrays / Minimig.ca

Sheet: /Power and programmable logic/ATX supply, front panel and status/

File: atx_power.kicad_sch

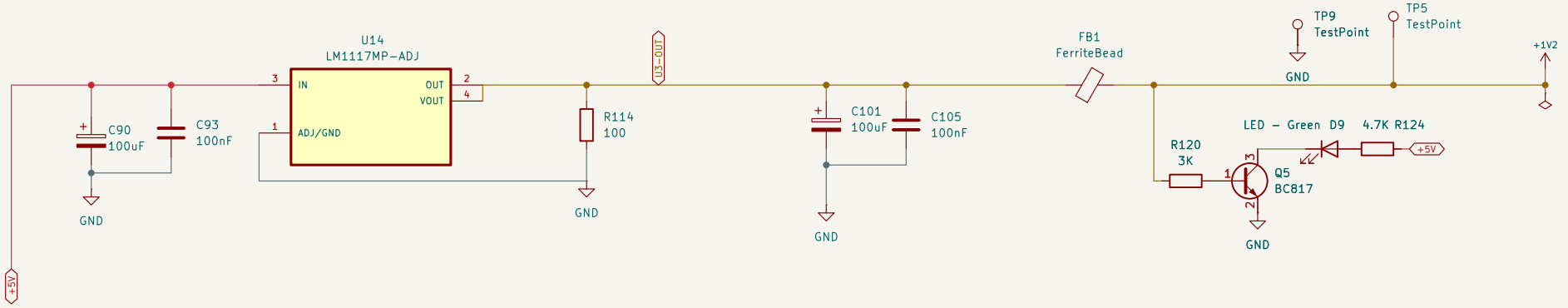
Title: MIST ITX / sheet 4

Size: A4 | Date: 2026-10-16 | Rev: V1R9

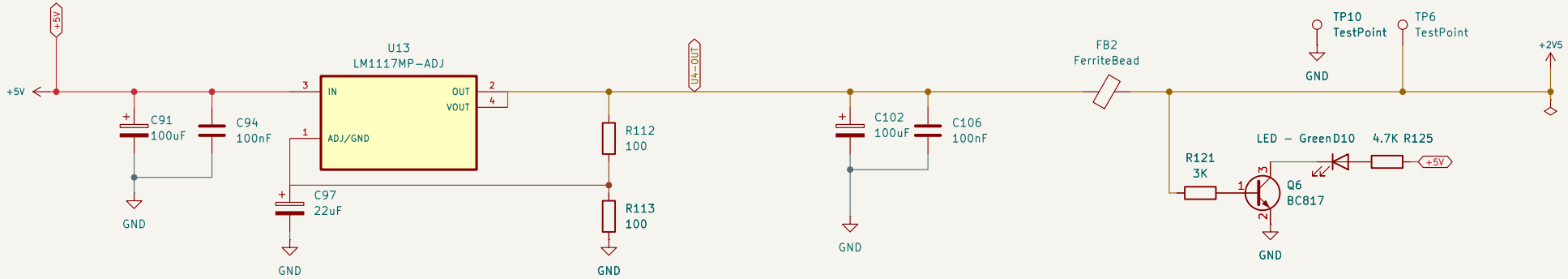
KiCad E.D.A. 10.0.7 | Id: 4/23

Core and auxiliary supplies

FPGA core supply



FPGA auxiliary supply



{B_CORE_AUX_POWER}

BUS {B_CORE_AUX_POWER}

+1V2, +2V5, +5V, GND

Precision-Arrays / Minimig.ca

Sheet: /Power and programmable logic/Core and auxiliary supplies/
File: core_aux_power.kicad_sch

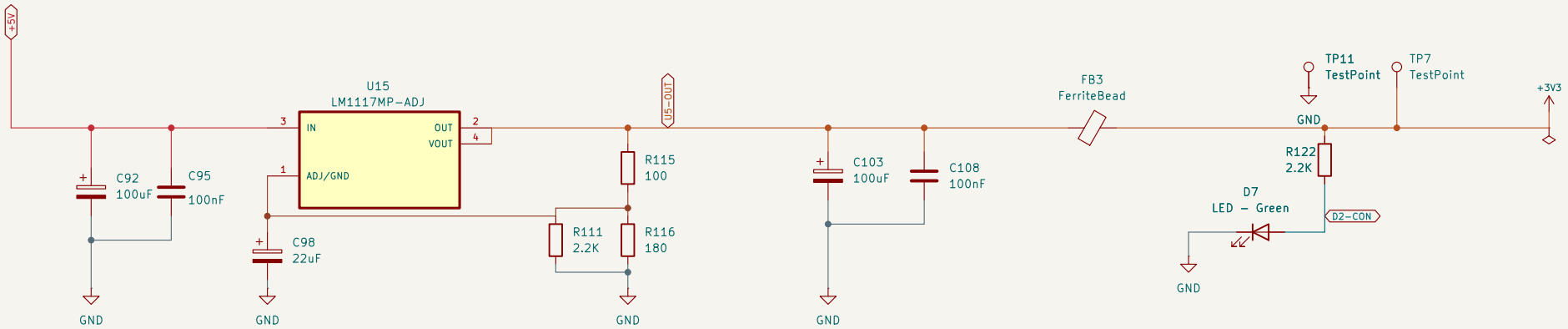
Title: MIST ITX / sheet 5

Size: A4 | Date: 2026-10-16 | Rev: V1R9

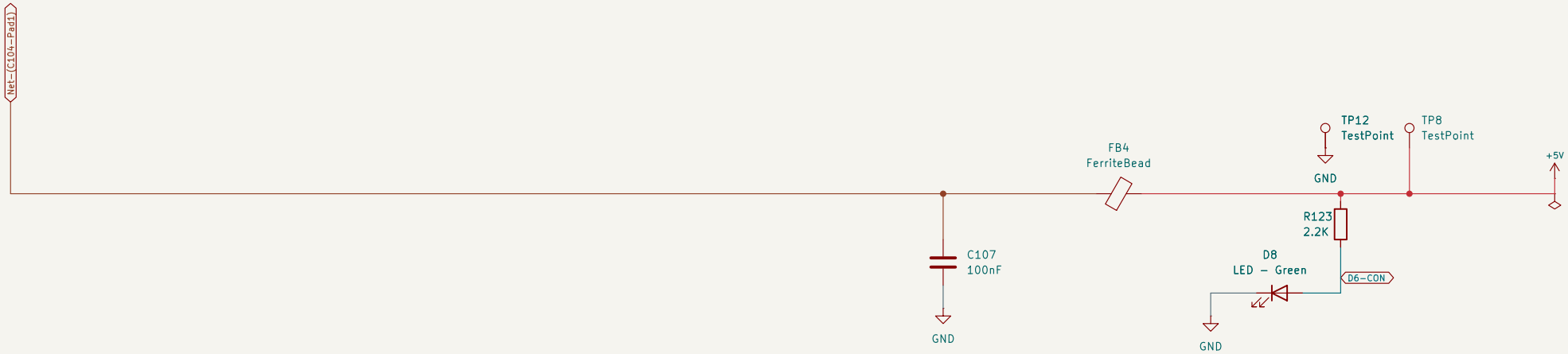
KiCad E.D.A. 10.0.7 | Id: 5/23

3.3 V and 5 V supplies

3.3 V logic supply



5 V rail and filtering



{B_LOGIC_POWER}

BUS {B_LOGIC_POWER}

+3V3, +5V, GND, Net-(C104-Pad1)

Precision-Arrays / Minimig.ca

Sheet: /Power and programmable logic/3.3 V and 5 V supplies/

File: logic_power.kicad_sch

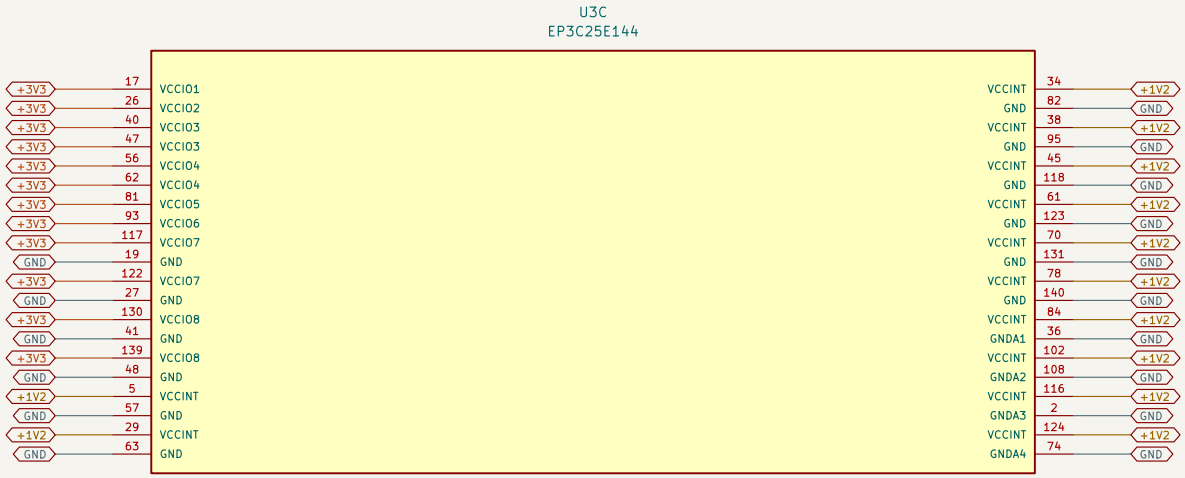
Title: MIST ITX / sheet 6

Size: A4 | Date: 2026-10-16 | Rev: V1R9

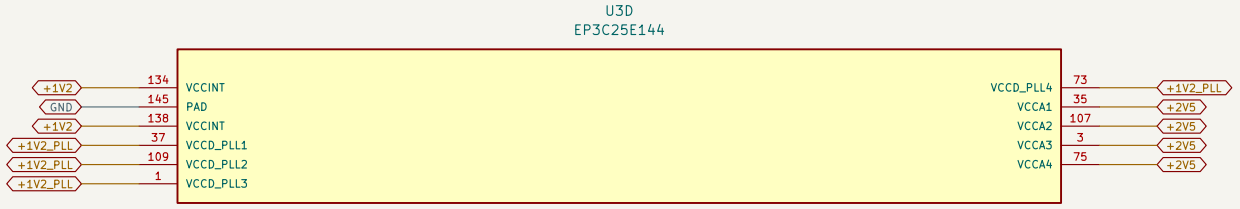
KiCad E.D.A. 10.0.7 | Id: 6/23

FPGA power units

Cyclone III – power / 1



Cyclone III – power / 2



{B_FPGA_POWER}

BUS {B_FPGA_POWER}

+1V2, +1V2_PLL, +2V5, +3V3, GND

Precision–Arrays / Minimig.ca

Sheet: /Power and programmable logic/FPGA power units/
File: fpga_power.kicad_sch

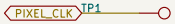
Title: MIST ITX / sheet 7

Size: A4	Date: 2026-10-16	Rev: V1R9
KiCad E.D.A. 10.0.7		Id: 7/23

FPGA support and decoupling

Cyclone III discrete support

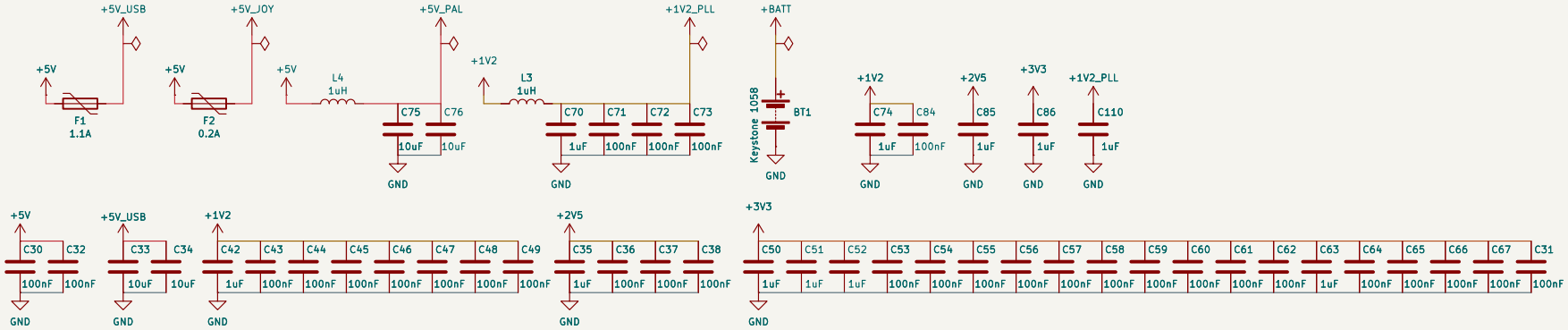








Power flags and decoupling



{B_FPGA_SUPPORT}

BUS {B_FPGA_SUPPORT}

+1V2, +1V2_PLL, +2V5, +3V3, +5V, +5V_JOY, +5V_PAL, +5V_USB, +BATT, CLK_27, GND, Net-(U3-CLK8/DIFFCLK_5n), Net-(U3-CLK12/DIFFCLK_7n), Net-(U3-CLK13/DIFFCLK_7p), Net-(U3-nCE), PIXEL_CLK, SCK

Precision-Arrays / Minimig.ca

Sheet: /Power and programmable logic/FPGA support and decoupling/
File: fpga_support.kicad_sch

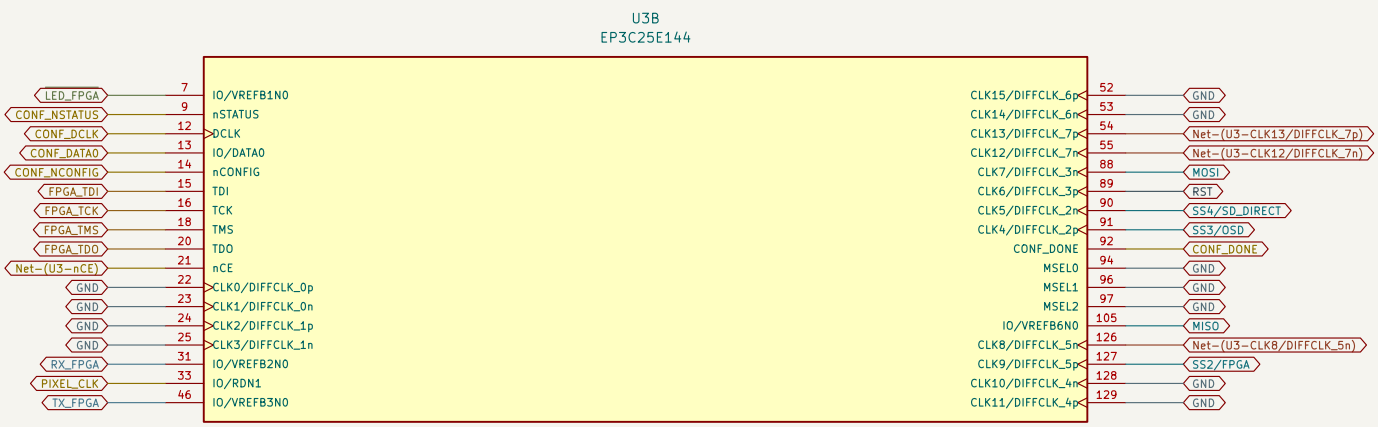
Title: MIST ITX / sheet 8

Size: A4 | Date: 2026-10-16 | Rev: V1R9

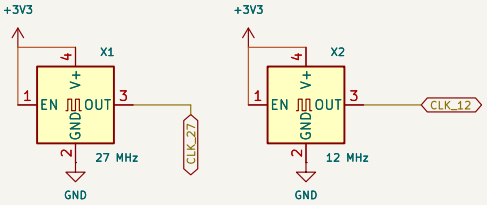
KiCad E.D.A. 10.0.7 | Id: 8/23

FPGA configuration, clocks and JTAG

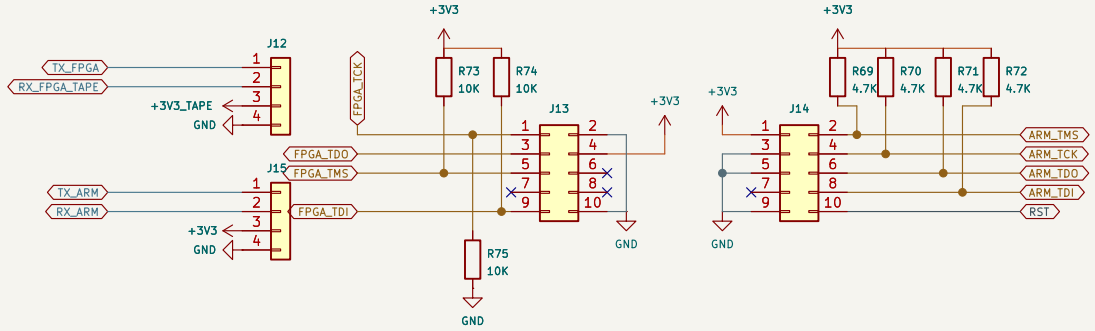
Cyclone III — control



System clocks



JTAG and debug



{B_FPGA_CONTROL}

BUS {B_FPGA_CONTROL}

+3V3, +3V3_TAPE, ARM_TCK, ARM_TDI, ARM_TDO, ARM_TMS, CLK_12, CLK_27, CONF_DATA0, CONF_DCLK, CONF_DONE, CONF_NCONFIG, CONF_NSTATUS, GND, MISO, MOSI, Net-(U3-CLK8/DIFFCLK_5n), Net-(U3-CLK12/DIFFCLK_7n), Net-(U3-CLK13/DIFFCLK_7p), Complete members: open the bus alias or documentation/index.html.

Precision-Arrays / Minimig.ca

Sheet: /Power and programmable logic/FPGA configuration, clocks and JTAG/
File: fpga_control.kicad_sch

Title: MIST ITX / sheet 9

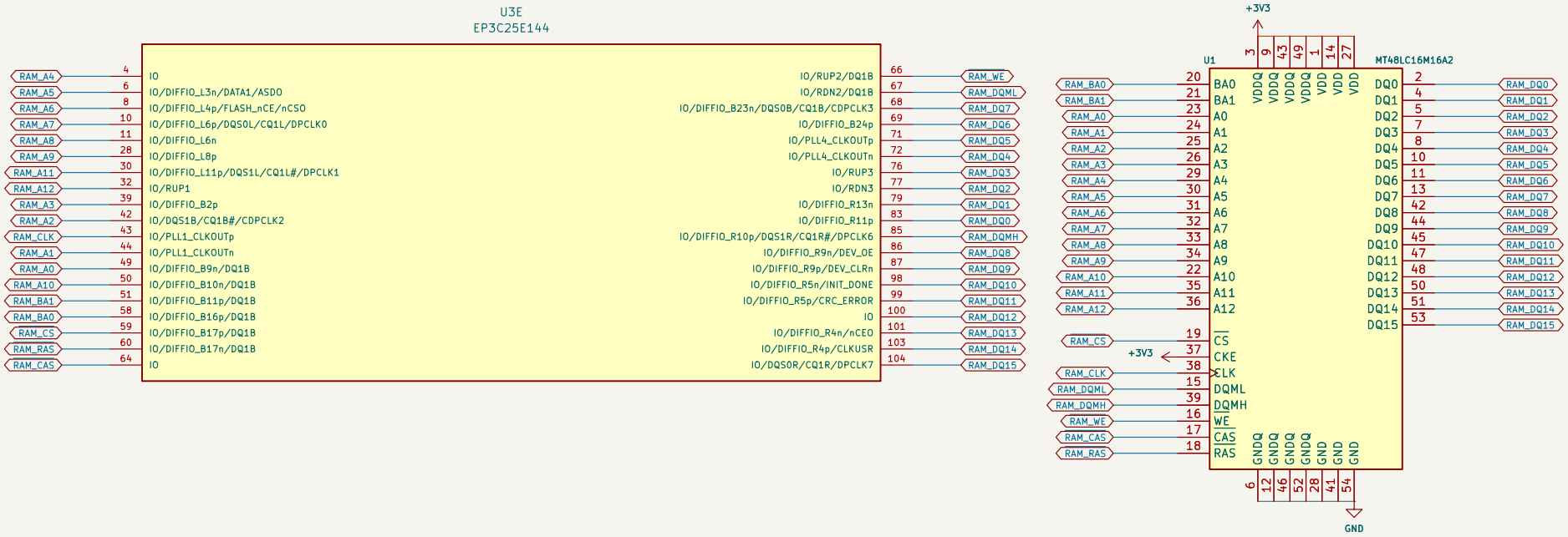
Size: A4 | Date: 2026-10-16 | Rev: V1R9

KiCad E.D.A. 10.0.7 | Id: 9/23

FPGA SDRAM interface and memory

Cyclone III — sdram

SDRAM memory



{B_MEMORY}

BUS {B_MEMORY}

+3V3, GND

Precision—Arrays / Minimig.ca

Sheet: /Power and programmable logic/FPGA SDRAM interface and memory/
File: memory.kicad_sch

Title: MIST ITX / sheet 10

Size: A4 | Date: 2026-10-16 | Rev: V1R9

KiCad E.D.A. 10.0.7 | Id: 10/23

Controllers and interfaces

ARM controller and USB programming

Sheet 12

{B_CONTROLLER} {B_CONTROLLER}

FPGA video, VGA and PAL encoding

Sheet 13

{B_VIDEO} {B_VIDEO}

FPGA audio and tape interface

Sheet 14

{B_SOUND} {B_SOUND}

Joysticks, buttons and serial selection

Sheet 15

{B_USER_IO} {B_USER_IO}

MIDI, RTC and WiFi expansion

Sheet 16

{B_MIDI_RTC} {B_MIDI_RTC}

USB host controller, hub and ports

Sheet 17

{B_USB_HOST} {B_USB_HOST}

Hierarchical buses name the cross-sheet signals. Global labels continue each exact native net.

Open documentation/index.html for the board guide, connector maps and validation records.

{B_CIRCUITS2}

BUS {B_CIRCUITS2}

B_CONTROLLER, B_VIDEO, B_SOUND, B_USER_IO, B_MIDI_RTC, B_USB_HOST

Precision-Arrays / Minimig.ca

Sheet: /Controllers and interfaces/
File: Circuits2.kicad_sch

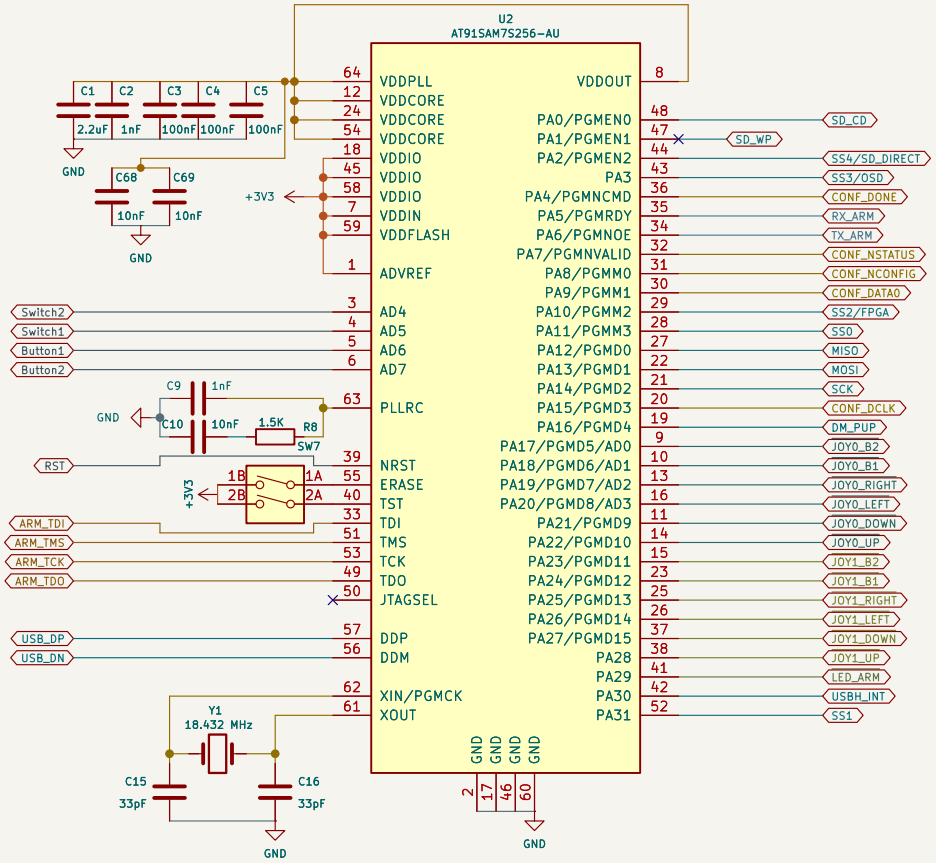
Title: MIST ITX / sheet 11

Size: A4 | Date: 2026-10-16 | Rev: V1R9

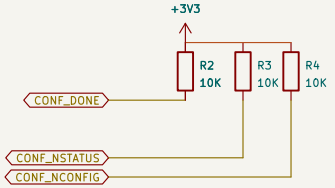
KiCad E.D.A. 10.0.7 | Id: 11/23

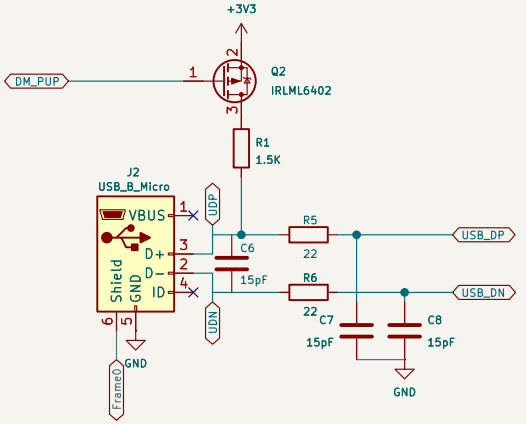
ARM controller and USB programming

ARM controller and support



ARM USB programming





{B_CONTROLLER}

BUS {B_CONTROLLER}

+3V3, ARM_TCK, ARM_TDI, ARM_TDO, ARM_TMS, Button1, Button2, CONF_DATA0, CONF_DCLK, CONF_DONE, CONF_NCONFIG, CONF_NSTATUS, Frame0, GND, MISO, MOSI, RST, RX_ARM, SCK, SD_CD, SS0, SS1, SS2/FPGA, SS3/OSD, SS4/SD_DIRECT, Switch1,
Complete members: open the bus alias or documentation/index.html.

Precision—Arrays / Minimig.ca

Sheet: /Controllers and interfaces/ARM controller and USB programming/
File: controller.kicad_sch

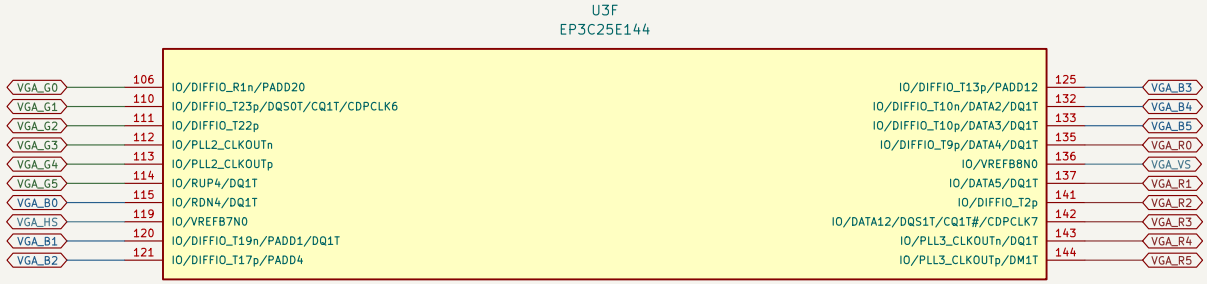
Title: MIST ITX / sheet 12

Size: A4 | Date: 2026-10-16 | Rev: V1R9

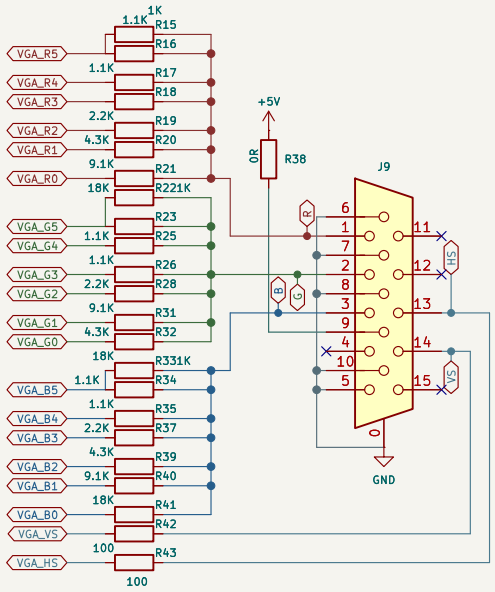
KiCad E.D.A. 10.0.7 | Id: 12/23

FPGA video, VGA and PAL encoding

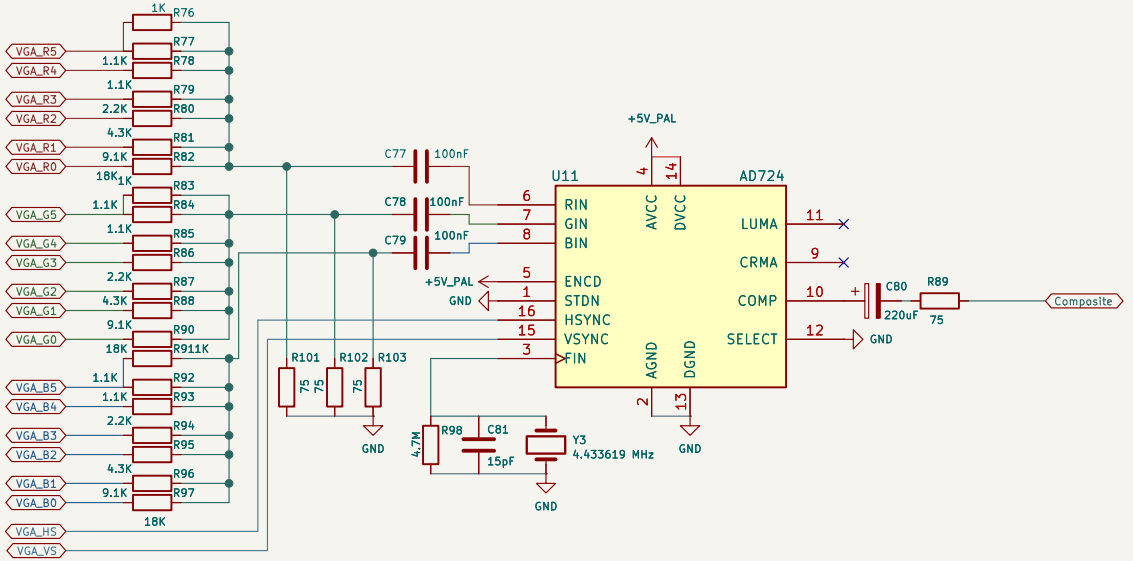
Cyclone III – video



VGA DAC and sync



PAL composite video encoder



{B_VIDEO}

BUS {B_VIDEO}

+5V, +5V_PAL, Composite, GND

Precision–Arrays / Minimig.ca

Sheet: /Controllers and interfaces/FPGA video, VGA and PAL encoding/
File: video.kicad_sch

Title: MIST ITX / sheet 13

Size: A4 | Date: 2026-10-16 | Rev: V1R9

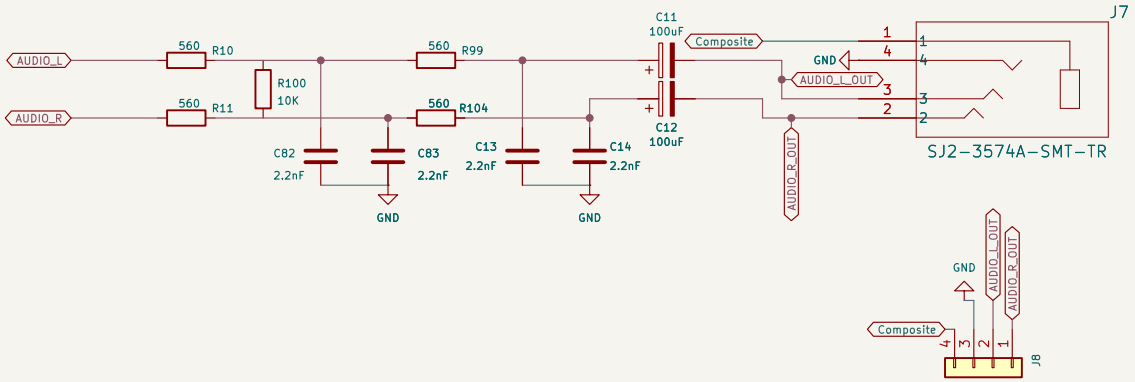
KiCad E.D.A. 10.0.7 | Id: 13/23

FPGA audio and tape interface

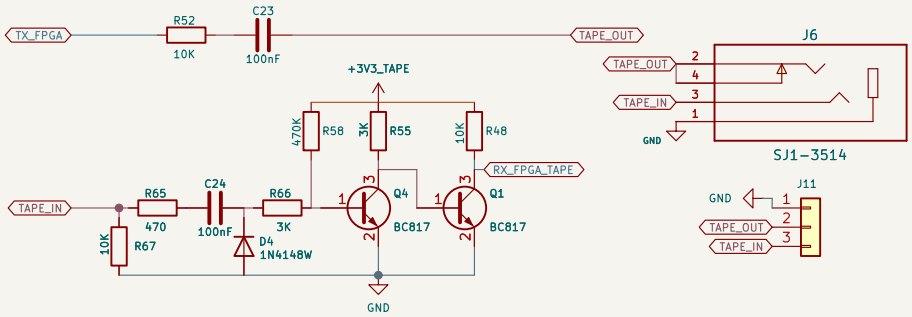
Cyclone III – audio



Audio and AV output



Tape interface



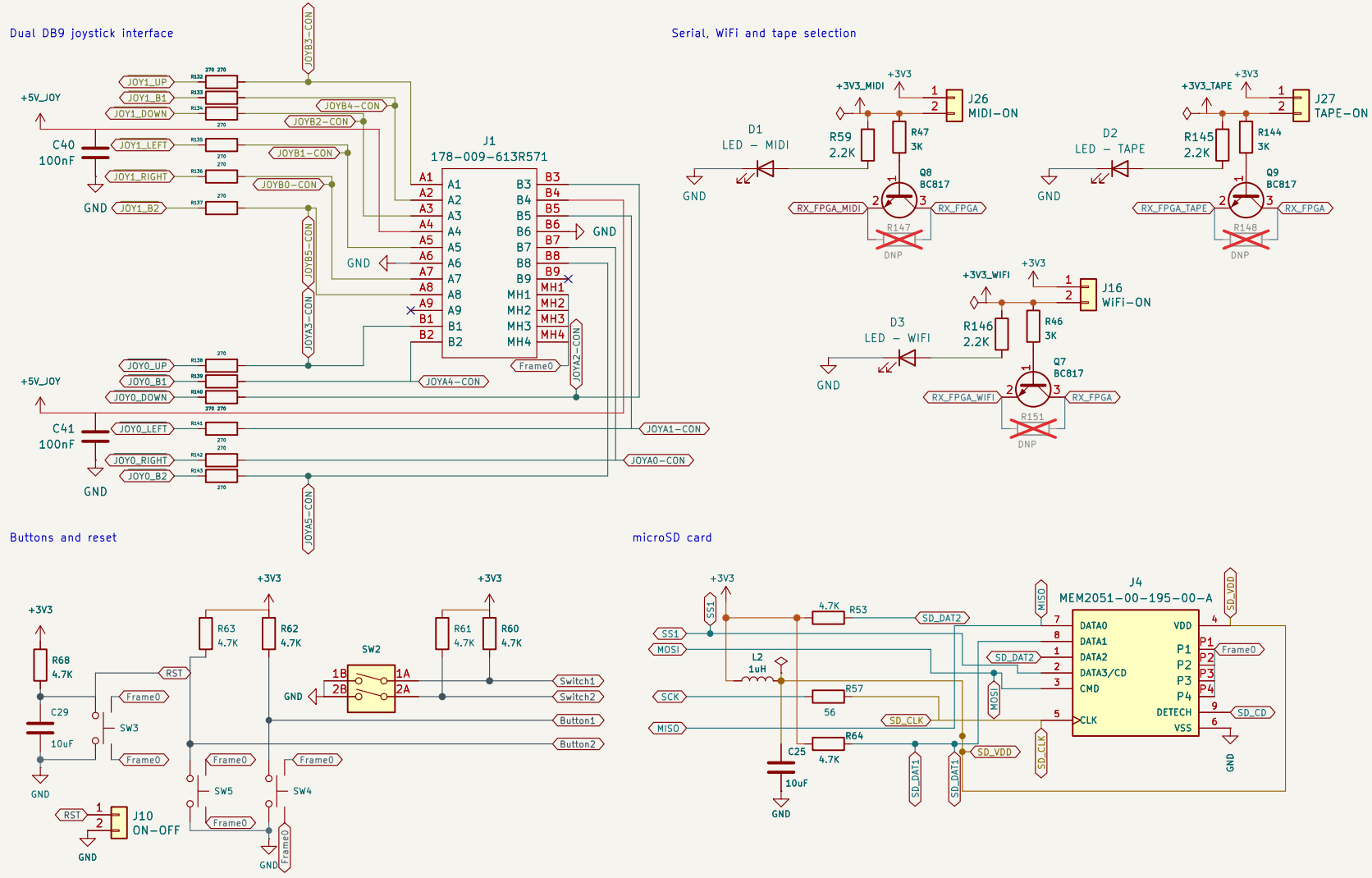
{B_SOUND}

BUS {B_SOUND}

+3V3_TAPE, Composite, GND, RX_FPGA_TAPE, TX_FPGA

Precision–Arrays / Minimig.ca	
Sheet: /Controllers and interfaces/FPGA audio and tape interface/ File: sound.kicad_sch	
Title: MIST ITX / sheet 14	
Size: A4	Date: 2026-10-16
KiCad E.D.A. 10.0.7	Id: 14/23
	Rev: V1R9

Joysticks, buttons and serial selection



{B_USER_IO}

BUS {B_USER_IO}

+3V3, +3V3_MIDI, +3V3_TAPE, +3V3_WIFI, +5V_JOY, Button1, Button2, Frame0, GND, MISO, MOSI, RST, RX_FPGA, RX_FPGA_MIDI, RX_FPGA_TAPE, RX_FPGA_WIFI, SCK, SD_CD, SS1, Switch1, Switch2, JOY0_B1, JOY0_B2, JOY0_DOWN, JOY0_LEFT, Complete members: open the bus alias or documentation/index.html.

Precision-Arrays / Minimig.ca

Sheet: /Controllers and interfaces/Joysticks, buttons and serial selection/
File: user_io.kicad_sch

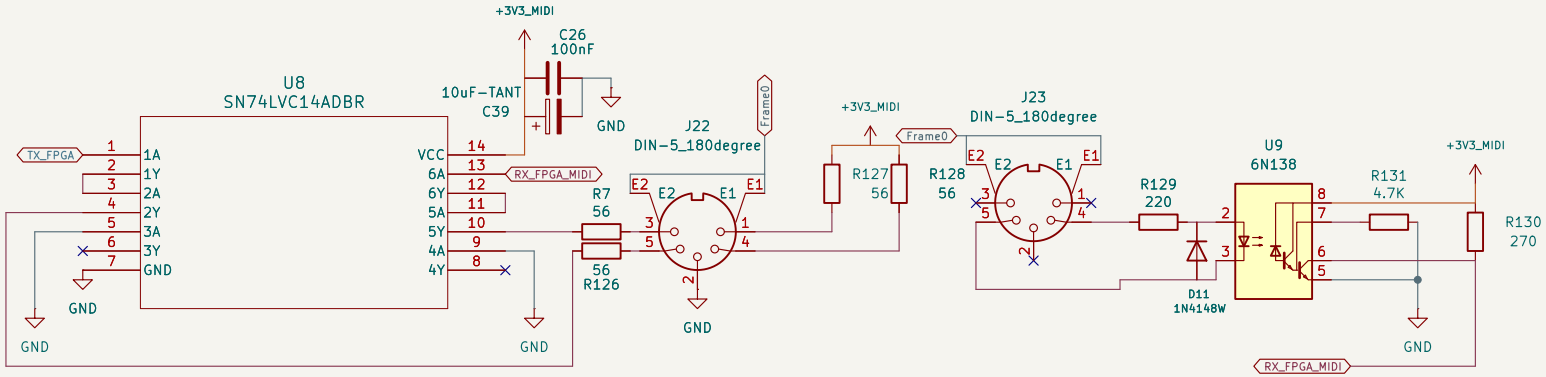
Title: MIST ITX / sheet 15

Size: A4 | Date: 2026-10-16 | Rev: V1R9

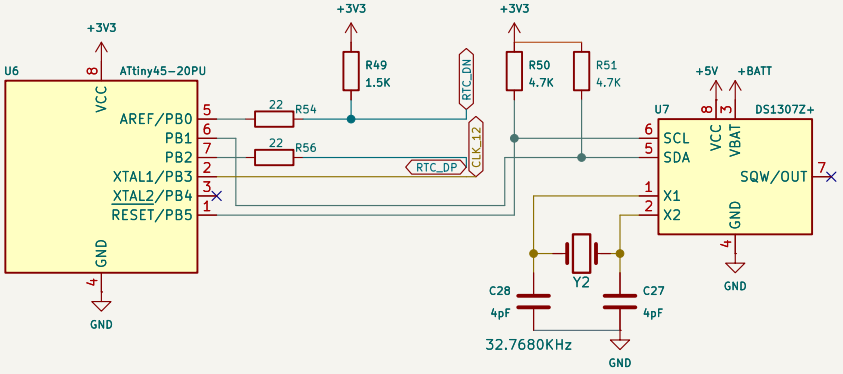
KiCad E.D.A. 10.0.7 | Id: 15/23

MIDI, RTC and WiFi expansion

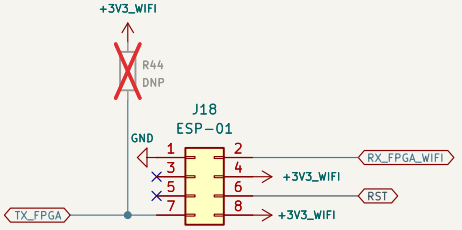
MIDI interface



RTC controller and battery



ESP-01 expansion



{B_MIDI_RTC}

BUS {B_MIDI_RTC}

+3V3, +3V3_MIDI, +3V3_WIFI, +5V, +BATT, CLK_12, Frame0, GND, RST, RTC_DN, RTC_DP, RX_FPGA_MIDI, RX_FPGA_WIFI, TX_FPGA

Precision-Arrays / Minimig.ca

Sheet: /Controllers and interfaces/MIDI, RTC and WiFi expansion/
File: midi_rtc.kicad_sch

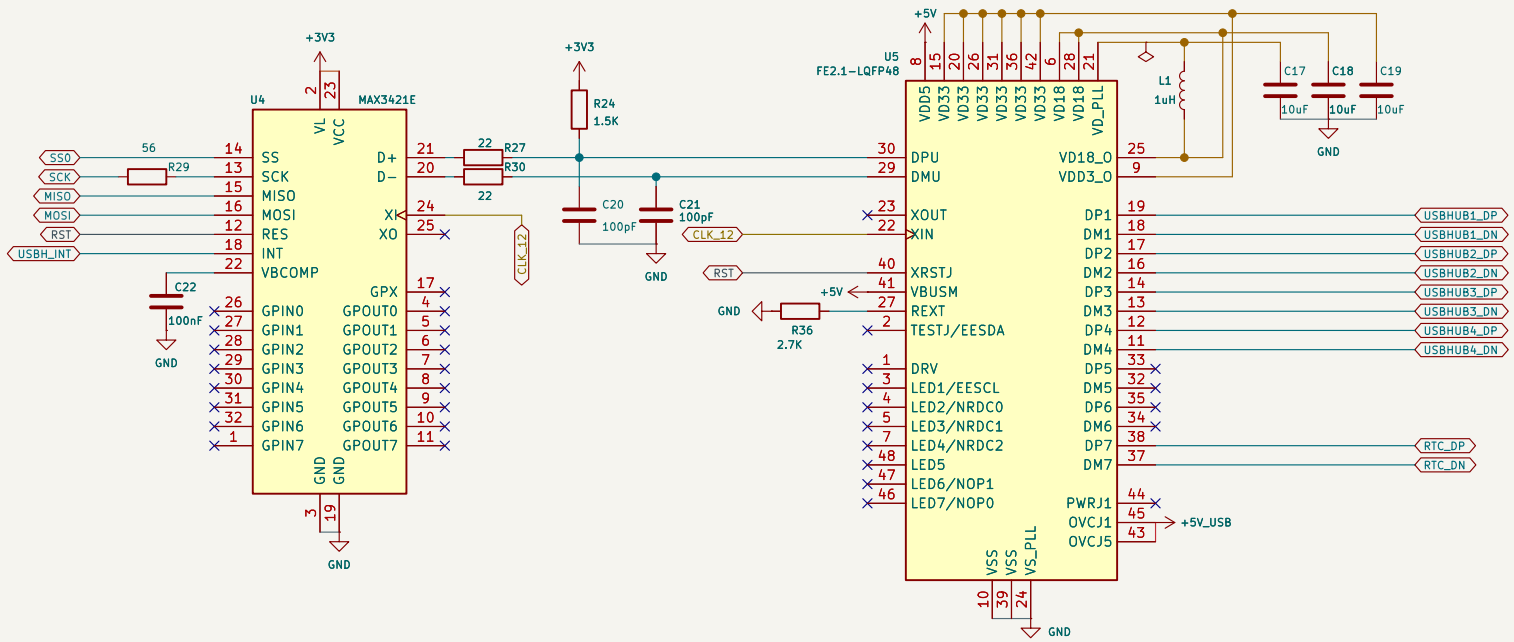
Title: MIST ITX / sheet 16

Size: A4 | Date: 2026-10-16 | Rev: V1R9

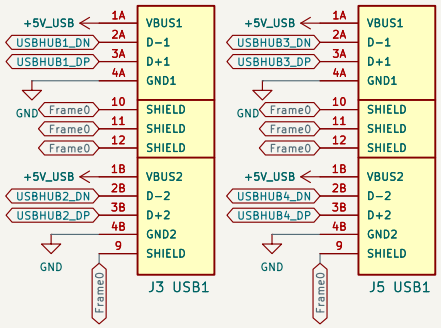
KiCad E.D.A. 10.0.7 | Id: 16/23

USB host controller, hub and ports

USB host controller and hub



USB host connectors



{B_USB_HOST}

BUS {B_USB_HOST}

+3V3, +5V, +5V_USB, CLK_12, Frame0, GND, MISO, MOSI, RST, RTC_DN, RTC_DP, SCK, SS0, USBH_INT

Precision—Arrays / Minimig.ca

Sheet: /Controllers and interfaces/USB host controller, hub and ports/
File: usb_host.kicad_sch

Title: MIST ITX / sheet 17

Size: A4	Date: 2026-10-16	Rev: V1R9
KiCad E.D.A. 10.0.7		Id: 17/23

Board guide and engineering reference

Top assembly

Sheet 19

Bottom assembly

Sheet 20

Layer stackup and fabrication

Sheet 21

Routing guide

Sheet 22

Power and signal identification

Sheet 23

Hierarchical buses name the cross-sheet signals. Global labels continue each exact native net.

Open documentation/index.html for the board guide, connector maps and validation records.

Precision-Arrays / Minimig.ca

Sheet: /Board guide and engineering reference/
File: Documentation.kicad_sch

Title: MIST ITX / sheet 18

Size: A4 | Date: 2026-10-16 | Rev: V1R9

KiCad E.D.A. 10.0.7 | Id: 18/23

Top assembly

Component placement, fitted-side orientation and 3D reference

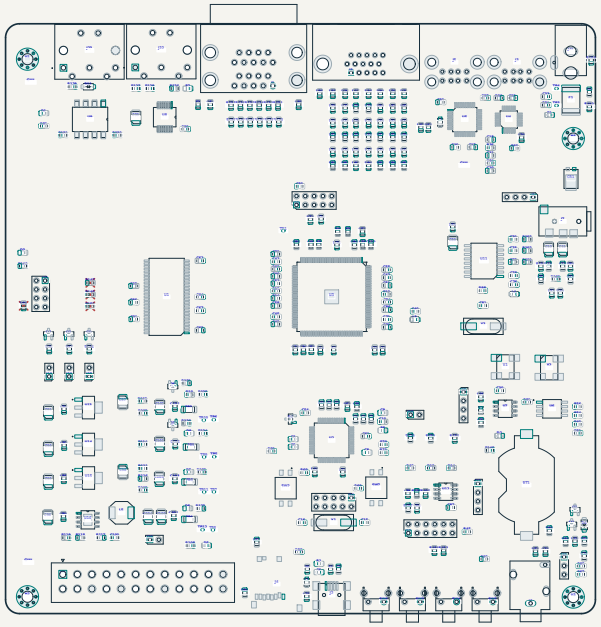
ASSEMBLY NOTES

01 View from outside the top of the board. Use connector edges to orient the board.

02 Teal identifies pad 1 / A1. Red crosses mark DNP footprints. Confirm polarity from the footprint and datasheet.

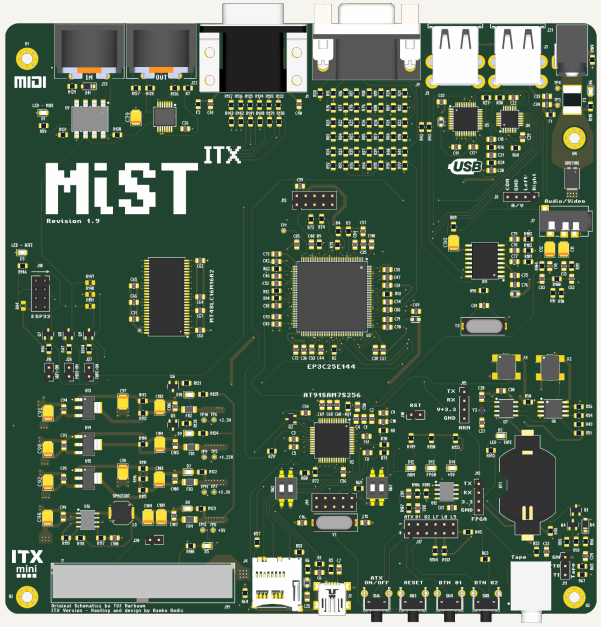
03 The component table controls values and population. The 3D view is illustrative; use the scale below for the plan.

REFERENCE PLAN



25 mm scale check / plan 0.46:1

3D ASSEMBLY VIEW



170.00 × 170.00 mm outline

ASSEMBLY INVENTORY

Placement	Footprints	SMD	DNP
Top side	369	325	4
Bottom side	2	0	0

Saved pads and fabrication outlines form the reference plan. Component values, connector pin maps and source notes are in documentation/index.html.

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V1R9 • generated 2026-10-16 • source a0bd5dacd4aa

Units: mm. Source CAD governs. Regenerate after design changes.

Documentation only; no electrical symbols

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Sheet: /Board guide and engineering reference/Top assembly/
File: AssemblyTop.kicad_sch

Title: MIST ITX / Top assembly

Size: A4	Date: 2026-10-16	**Rev: V1R9**
KiCad E.D.A. 10.0.7		Id: 19/23

Bottom assembly

Component placement, fitted-side orientation and 3D reference

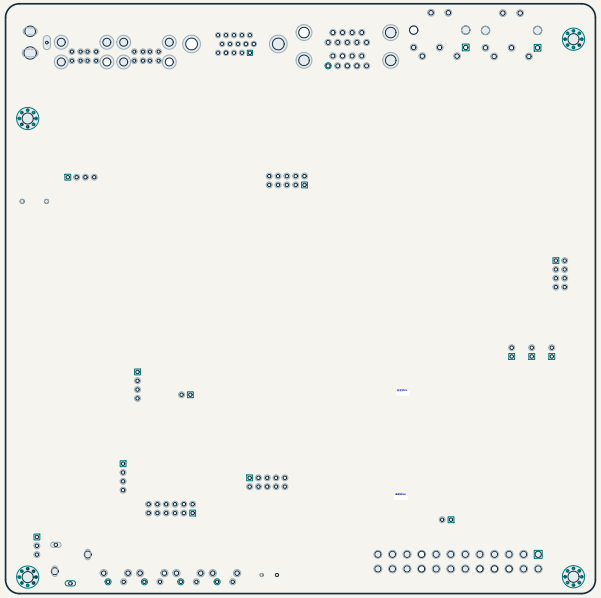
ASSEMBLY NOTES

01 View from outside the bottom of the board. Bottom plan is mirrored.

02 Teal identifies pad 1 / A1. Red crosses mark DNP footprints. Confirm polarity from the footprint and datasheet.

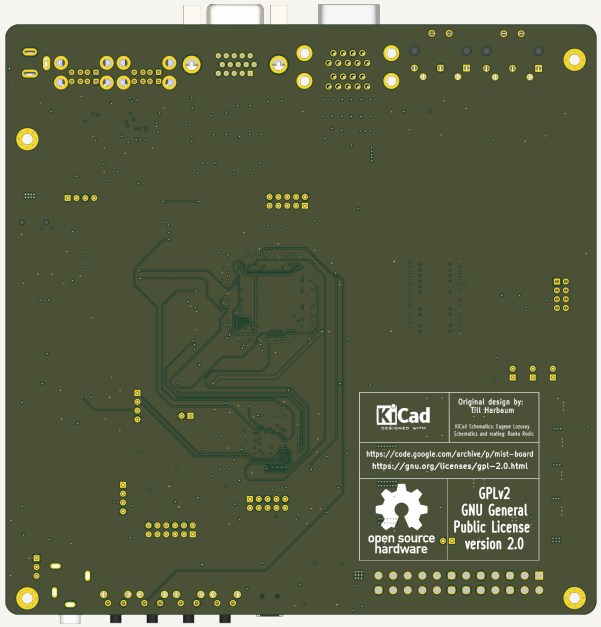
03 The component table controls values and population. The 3D view is illustrative; use the scale below for the plan.

REFERENCE PLAN



25 mm scale check / plan 0.46:1

3D ASSEMBLY VIEW



170.00 × 170.00 mm outline

ASSEMBLY INVENTORY

Placement	Footprints	SMD	DNP
Top side	369	325	4
Bottom side	2	0	0

Saved pads and fabrication outlines form the reference plan. Component values, connector pin maps and source notes are in documentation/index.html.

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Sheet: /Board guide and engineering reference/Bottom assembly/
File: AssemblyBottom.kicad_sch

Title: MIST ITX / Bottom assembly

Size: A4	Date: 2026-10-16	**Rev: V1R9**
KiCad E.D.A. 10.0.7		Id: 20/23

Layer stackup and fabrication

Source project settings. Dimensions and fabrication parameters come from the saved PCB.

Layer	Type	Material	mm
F.SilkS	Top Silk Screen	—	—
F.Paste	Top Solder Paste	—	—
F.Mask	Top Solder Mask	—	0.01
F.Cu	copper	—	0.035
dielectric 1	core	FR4	0.1
In1.Cu	copper	—	0.035
dielectric 2	core	FR4	0.535
In2.Cu	copper	—	0.035
dielectric 3	prepreg	FR4	0.1
In3.Cu	copper	—	0.035
dielectric 4	core	FR4	0.535
In4.Cu	copper	—	0.035
dielectric 5	prepreg	FR4	0.1
B.Cu	copper	—	0.035
B.Mask	Bottom Solder Mask	—	0.01
B.Paste	Bottom Solder Paste	—	—
B.SilkS	Bottom Silk Screen	—	—

Saved board parameters

Property	Saved value
Outline	170.00 × 170.00 mm
Board thickness	1.6 mm
Copper layers	6
Footprints	371
Track/arc items	3961
Vias	608

Saved routing rules / mm

Class	Clearance	Track	Via/drill
Default	0.2	0.2	0.6/0.3

These drawings record the source design. Confirm material, layer stack and fabrication capabilities against the native project before manufacture.

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Units: mm. Source CAD governs. Regenerate after design changes.

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Sheet: /Board guide and engineering reference/Layer stackup and fabrication/
File: Stackup.kicad_sch

Title: MIST ITX / Layer stackup and fabrication

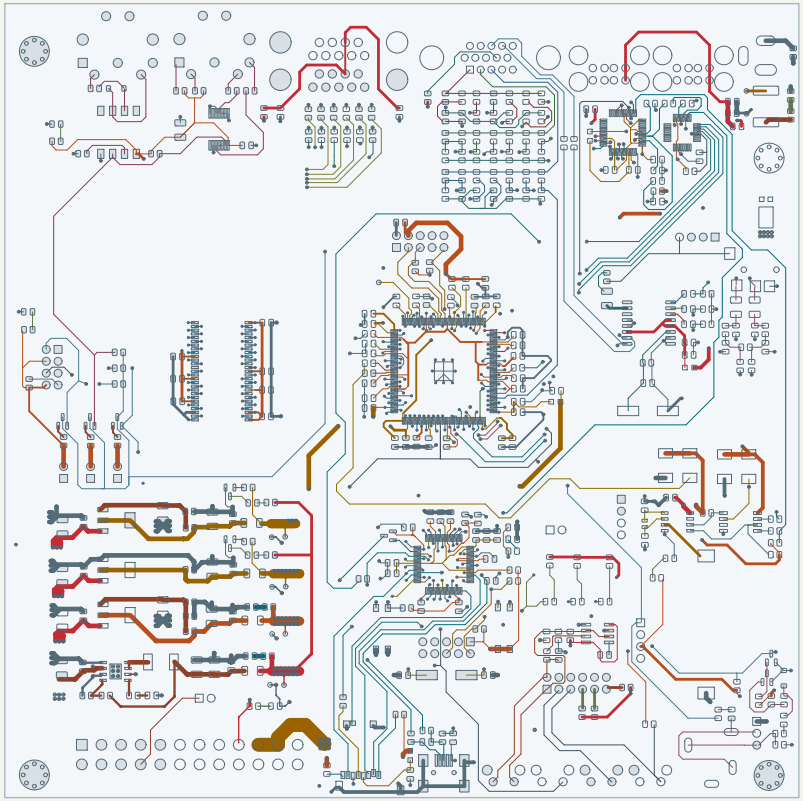
Size: A4 | Date: 2026-10-16 | Rev: V1R9

KiCad E.D.A. 10.0.7 | Id: 21/23

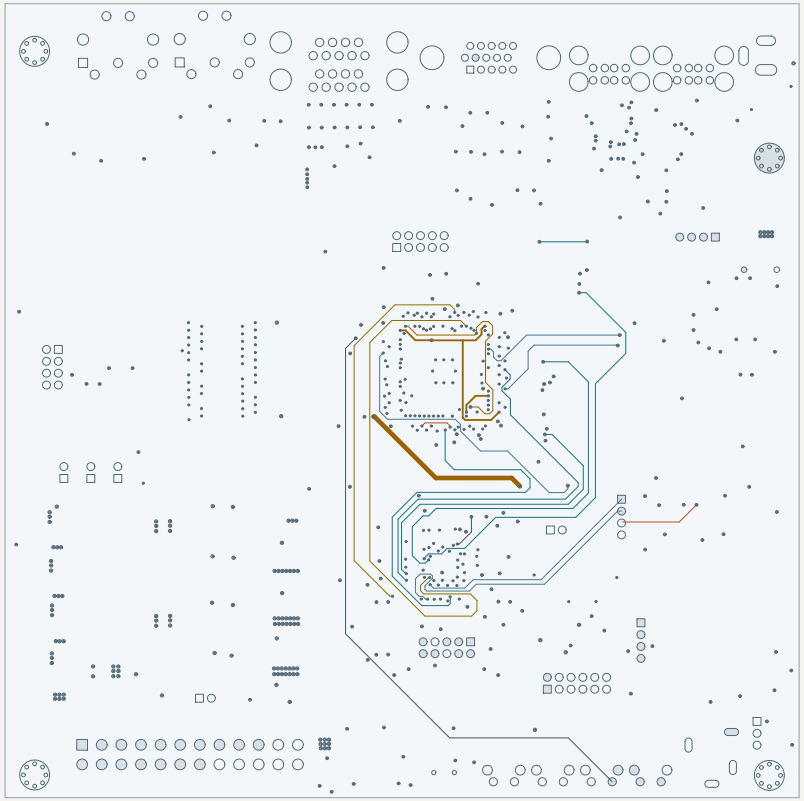
Routing guide

Outer copper from saved tracks, pads and vias. Filled zones are omitted for clarity.

Front copper



Back copper / through-board view



Colours identify net function. Grey pads and vias retain the saved geometry. Use native PCB layers for inner copper, zone fills and fabrication output.

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Units: mm. Source CAD governs. Regenerate after design changes.

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Sheet: /Board guide and engineering reference/Routing guide/
File: Routing.kicad_sch

Title: MIST ITX / Routing guide

Size: A4	Date: 2026-10-16	**Rev: V1R9**
KiCad E.D.A. 10.0.7		Id: 22/23

Power and signal identification

Shared functional colour families for schematic labels and PCB copper.

GROUND	2		USB	26
POWER 5V	5		SPI	13
POWER 3V3	5		CONFIG	8
POWER OTHER	12		JTAG	8
POWER CONTROL	23		UART	6
CLOCK	9		MIDI	13
SDRAM	38		JOYSTICK 1	12
VIDEO RED	8		JOYSTICK 2	12
VIDEO GREEN	8		AUDIO	15
VIDEO BLUE	8		INDICATORS	16
VIDEO SYNC	4		RTC	4
VIDEO COMPOSITE	9		CONTROL	5

Follow each signal through the hierarchy by its global net label. Bus aliases summarize cross-sheet signal groups; the HTML guide lists every alias and colour assignment.

PCB Editor: Appearance → Objects → Net colours → All. Colour-only VIS_ classes preserve the original track, via and clearance rules.

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V1R9 • generated 2026-10-16 • source a0bd5dacd4aa

Units: mm. Source CAD governs. Regenerate after design changes.

Documentation only; no electrical symbols
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Sheet: /Board guide and engineering reference/Power and signal identification/
File: PowerAndBuses.kicad_sch
Title: MIST ITX / Power and signal identification
Size: A4 | Date: 2026-10-16 | Rev: V1R9
KiCad E.D.A. 10.0.7 | Id: 23/23