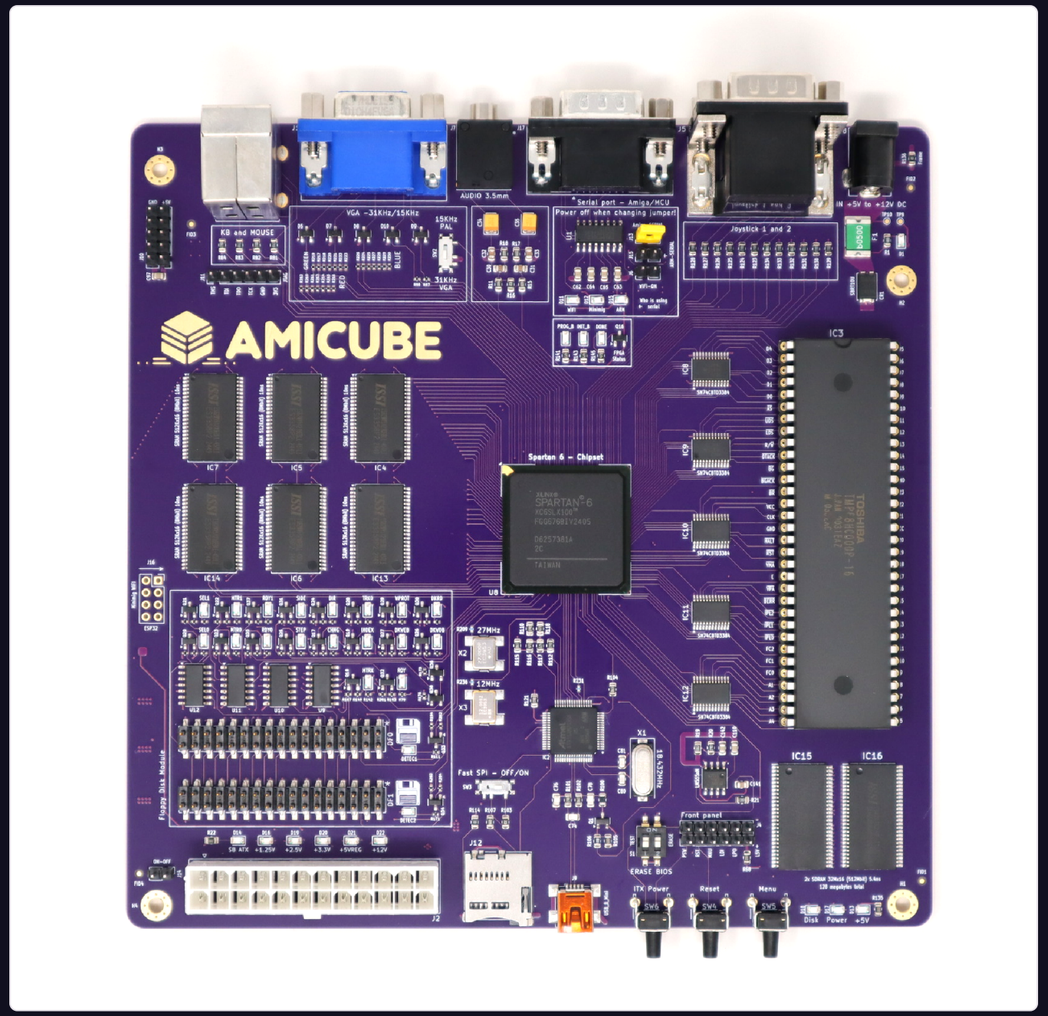
AMIGA SPIRIT. NEW POSSIBILITIES.

AmiCube v1.1

AGA colour. Real floppy disks.
A soft 020 and a real CPU socket.

128 MiB SDRAM | ARM + F12 | PICASSO96 RTG

Designed by Ranko Rodic · Minimig.ca



BUILT ON THE MINIMIG TRADITION

More colour. More memory. More ways to make it your own.

DISPLAY

AGA + RTG

Native Amiga graphics and a Picasso96 framebuffer for Workbench in supported configurations.

MEMORY

128 MiB SDRAM

Two 64 MiB SDRAM devices give the FPGA room for Chip RAM, Fast RAM and graphics buffers.

CONTROL

A new F12 experience

The physical ARM controller manages setup, disk images, hardfiles and empty ADF creation.

Keep the physical connections, the disk-drive sounds and the freedom to experiment.

From the original Minimig to AmiCube v1.1.

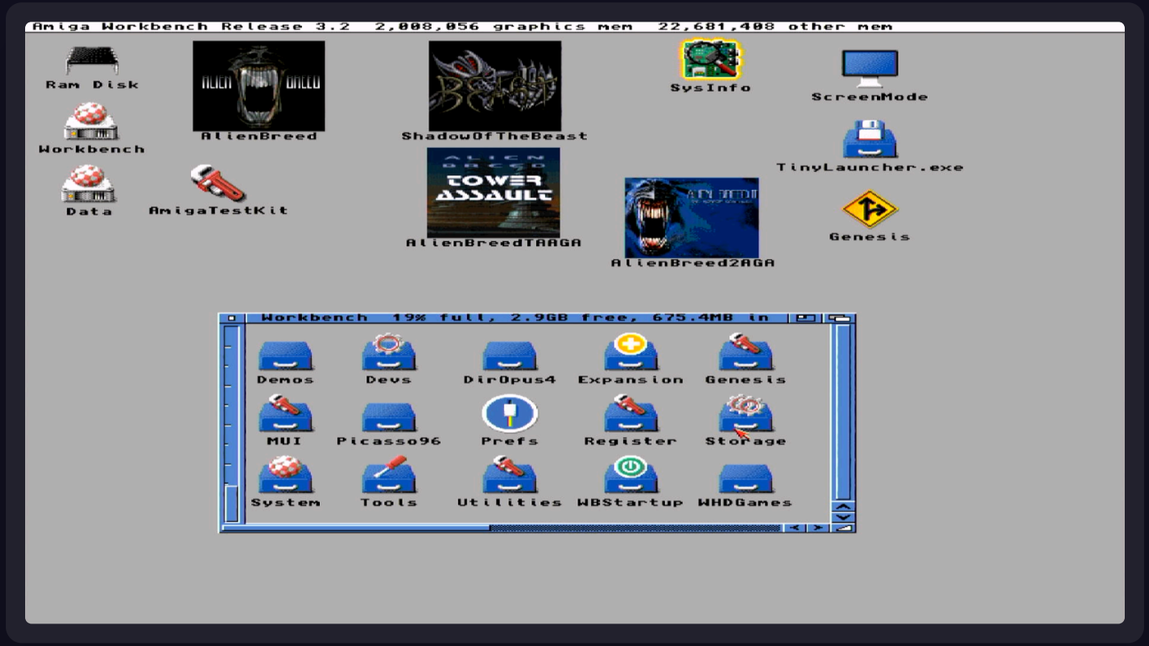
FEATURE	ORIGINAL MINIMIG	AMICUBE V1.1
Chipset	Original Amiga / OCS; later ECS cores	OCS / ECS / AGA with recent compatibility updates
FPGA	Spartan-3 XC3S400	Spartan-6 XC6SLX100
Memory	2 MB SRAM on the original board	128 MiB physical SDRAM; SOFT profile: 2 MiB Chip + 120 MiB Fast
Amiga CPU	Physical MC68SEC000	TG68 soft 020, or separate HARD core for the DIP64 socket
System control	PIC controller and image-selection OSD	Physical ARM + unified F12 menu + Create empty ADF
Floppy workflow	ADF images on flash media	Real DF0/DF1 or ADF; virtual DF2/DF3; physical copying
Graphics expansion	Native Amiga video	Native AGA plus Picasso96 RTG in supported configurations

Comparison uses the original 2 MB Minimig design, not later 4 MB / 6 MB Minimig boards or ARM upgrades. AmiCube's physical SDRAM total is not the same as usable Fast RAM.

ADVANCED GRAPHICS ARCHITECTURE

A little more AGA in your life.

Amiga colour, Copper effects and a living Workbench on modern FPGA hardware.



Hardware capture: Workbench 3.2 on an earlier SOFT/RTG profile. The screen's memory count belongs to that profile.

18-bit

ANALOGUE RGB DAC
6 BITS PER CHANNEL

RTG

PICASSO96
FRAMEBUFFER OUTPUT

The 18-bit DAC describes the physical RGB output precision. AGA's internal palette and the bit depth of an RTG mode are separate properties.

A soft 020.
A real socket. Your choice.

SOFT CORE

TG68 inside the FPGA

68020-class operation, guest-controlled cache and the SDRAM-backed Amiga memory map. LQ42 is the current board-tested SOFT release.

HARD / SOCKET CORE

Physical DIP64 CPU path

Dedicated FPGA builds support the external processor interface. Board records include 68SEC000, TF534 and PiStorm/PiStorm68K operation.

Both paths share the physical AT91SAM7S256 ARM controller and V11R1FA firmware.

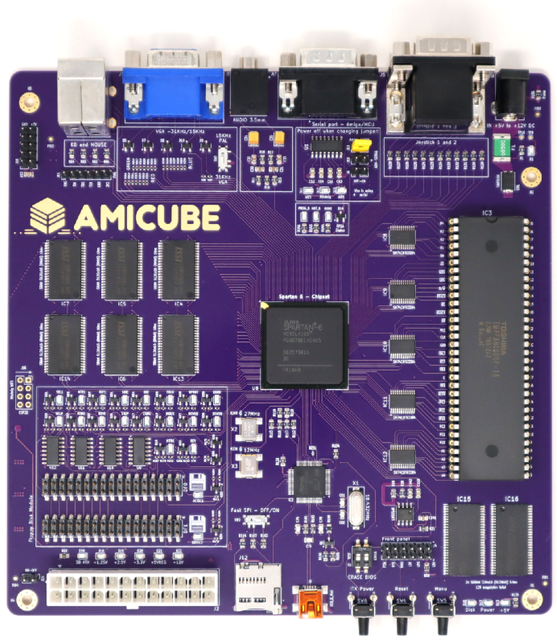
Select the appropriate FPGA boot image. This is a choice between separate cores; the PiStorm68K adapter has its own hardware CPU selector.

A MUCH LARGER PLAYGROUND

128 MiB. On the board.

Dual-rank SDRAM replaces the original Minimig's small SRAM-only memory architecture.

Two 64 MiB devices share one 16-bit bus, managed by the FPGA. The SOFT profile maps **2 MiB Chip + 120 MiB Fast RAM**, with optional Slow RAM.



2 MiB Chip	120 MiB Fast · SOFT profile	Other use

Illustrative allocation, not to scale. ROM, buffers, mapping and CPU/core selection affect available memory; the same Fast RAM total does not apply to every HARD configuration.

KEEP THE CLICK OF A REAL DRIVE

Real disks. Virtual disks. One machine.

DF0 and DF1 independently select a physical mechanism or an ADF image. DF2 and DF3 remain virtual image drives.

Recorded milestones include full physical DF0 → DF1 copying, ADF → physical copying and loading original media with the P112 reader.

> Use write-protected originals for reading and spare disks for write demonstrations.

Real hardware photo from the September 1 P112 milestone. Original-media results are tied to that tested build.

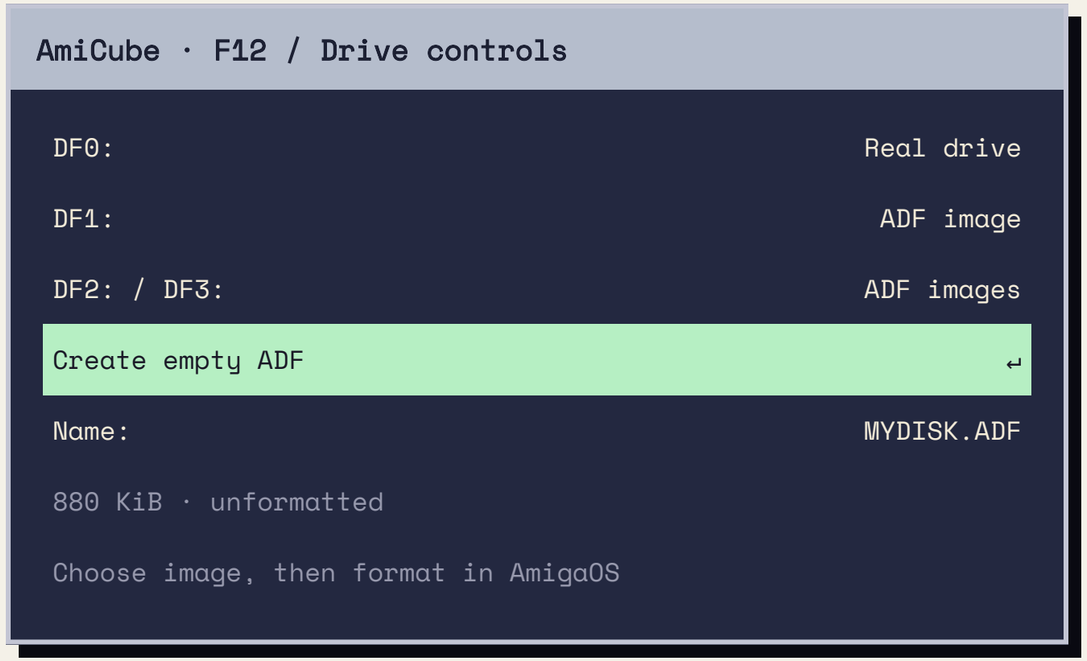
V11R1FA · PHYSICAL ARM CONTROLLER

A blank disk, without leaving the machine.

Create an empty ADF directly from F12.

Type 1–8 characters. The firmware adds .ADF, checks the name and available space, then writes an unformatted 880 KiB image to the SD root.

> Creation does not automatically mount or format the image.



Illustrated menu summary; layout simplified from the firmware controls.

01 / CREATE

Press F12

Choose “Create empty ADF” and enter a short name.

02 / SAVE

880 KiB on SD

The ARM creates an empty .ADF in the card’s root folder.

03 / INSERT

Pick your drive

Use the DFx image picker to mount the new file.

04 / USE

Format or copy

Format in AmigaOS, or use it as a disk-copy destination.

Your whole setup, one familiar key.

CONFIGURATION

CPU, chipset & memory

Choose CPU and chipset modes, RAM allocation and real/ADF drive ownership. Reset-sensitive choices are staged until an explicit reset.

STORAGE

Images & hardfiles

Select ADFs and HDFs. Supported backends include synthetic-RDB hardfiles, whole SD cards and populated primary MBR partitions.

DISPLAY & INPUT

RTG, scanlines & autofire

Control RTG permission, native video filtering, Off/50%/Black scanlines and persistent autofire.

One physical AT91SAM7S256 host, shared firmware for SOFT and HARD builds, and a unified indexed overlay on native and RTG output.

Full seven-button CD32 input, HDMI/scaler controls and HRTmon are not current advertised features. Core-specific controls depend on the selected build.

NEW MILESTONE · SEPTEMBER 9, 2026

PiStorm. Meet AmiCube RTG.

Workbench at 800 × 600, 16-bit colour.

HARD H8 confirms PiStorm operation with AmiCube's own Minimig/Picasso96 driver and native board display path.

> A hardware-confirmed development milestone. Broader regression testing and global timing closure remain open.

Photo: Ranko Rodic · HARD H8 cost043 · 9 September 2026.

A BIGGER FPGA. A MORE USEFUL DEVELOPMENT BOARD.

Spartan-6, with room for the whole machine.

101,261
LOGIC CELLS
XC6SLX100

4,824
KBIT BLOCK RAM
ON THE FPGA

180
DSP48A1 SLICES
DEVICE RESOURCES

12 / 27
MHz OSCILLATORS
DEVELOPMENT / MAIN

CLOCKING

New clock sources

The 27 MHz main source replaces the old 24 MHz generator. A separate 12 MHz oscillator provides a development clock.

OBSERVABILITY

See the FPGA status

Configuration/status LEDs help follow FPGA bring-up; the two floppy interfaces expose drive and signal activity.

MEMORY OPTIONS

SRAM stays on board

The six SRAM devices remain available for development and auxiliary uses alongside the new 128 MiB SDRAM system.

AMD Spartan-6 specifications ↗ AmiCube hardware baseline ↗

THE CHIPSET AND THE CPU HAVE DIFFERENT JOBS

AGA does not have to mean an 020-only machine.

PHYSICAL CPU

68000 + AGA

The HARD core supports physical 68000-family operation. AGA titles compiled for 68000 can run in a suitable setup; 020+ binaries still need the right CPU.

ACCELERATOR SOCKET

TF030-family experiments

The documented TF534 setup runs Zool 1 AGA. Socket-clock selections up to 60 MHz have working board records for specific CPU/accelerator combinations.

MEMORY PERFORMANCE

32-bit Chip RAM path

The FPGA's wider Chip RAM datapath and accelerated memory architecture support higher throughput. Actual performance depends on the core and configuration.

The soft CPU and HARD/socket variants both integrate physical-floppy support. Read original disks and move data between ADFs and real mechanisms.

60 MHz is a selected socket-clock setting in documented experiments, not a universal CPU rating. The physical SDRAM bus is 16-bit; the internal Chip RAM datapath is a separate width.

TF534 board record ↗ Physical 68000 results ↗

The connections are part of the experience.

VIDEO

18-bit RGB

VGA connector with 15 kHz / 31 kHz hardware selection for an appropriate display.

INPUT

Classic controls

PS/2 keyboard and mouse connections, plus two DB9 joystick ports.

MEDIA

Real drives + SD

Two physical floppy connectors, SD storage and familiar image workflows.

HARDWARE

A visible machine

Physical CPU socket, ARM controller, rail/status LEDs, ATX power connector and front-panel controls.

Build on Dennis van Weeren's Minimig foundation and the wider Minimig / MiST / Edge / TG68 community's work.

Board shown is the AmiCube v1.1 prototype. Hardware revisions, CPU adapters and core configurations have their own compatibility requirements.

WORLD OF RETRO COMPUTING EXPO 2026

Let’s talk Amiga hardware.

September 12–13 · 10 am–6 pm

Free admission · All ages

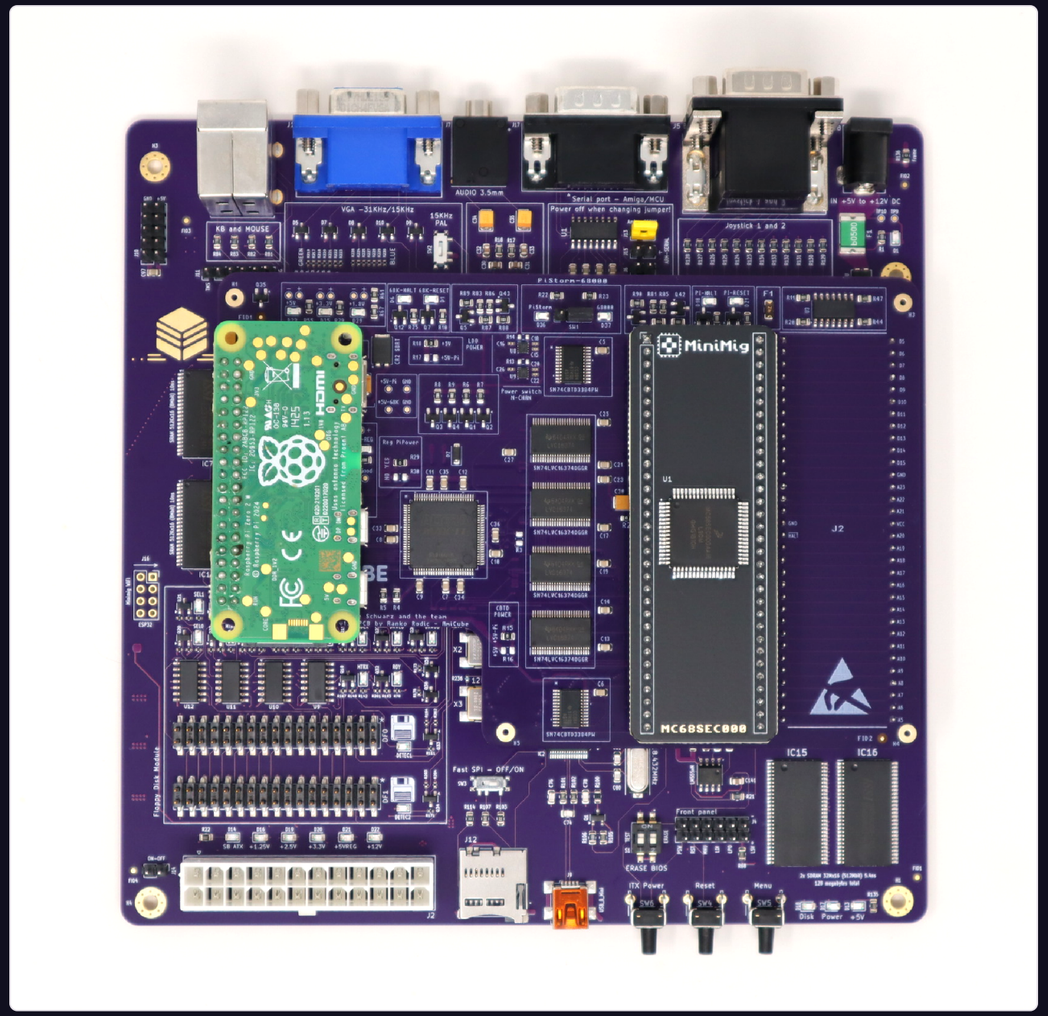
IDEAs Clinic, Room 1427

Pearl Sullivan Engineering / Engineering 7

University of Waterloo

263 Phillip Street, Waterloo, Ontario

MINIMIG.CA · PLATINUM SPONSOR



Built on real hardware. Developed, tested and refined.

Build records

AmiCube v1.1 development record
LQ42 SOFT working release · 8 September
V11R1FA: Create empty ADF
HARD H8: PiStorm RTG · 9 September
ARM OSD feature audit

Minimig heritage & event

Dennis van Weeren's original Minimig description
ACube original Minimig specifications
Official WoRC 2026 event information

Read the feature claims in context

Features depend on the selected FPGA core, firmware and CPU configuration. SOFT LQ42 is a board-tested working release; HARD socket cores remain in active development. Global timing closure remains open.

Photos document specific hardware milestones. Older demo photos and benchmark screens do not establish identical results for every later core.

No Kickstart ROMs, games or disk images are included. Product imagery: Ranko Rodic / Minimig.ca. Project credits include Dennis van Weeren, TG68, MiST/Minimig and Edge contributors.